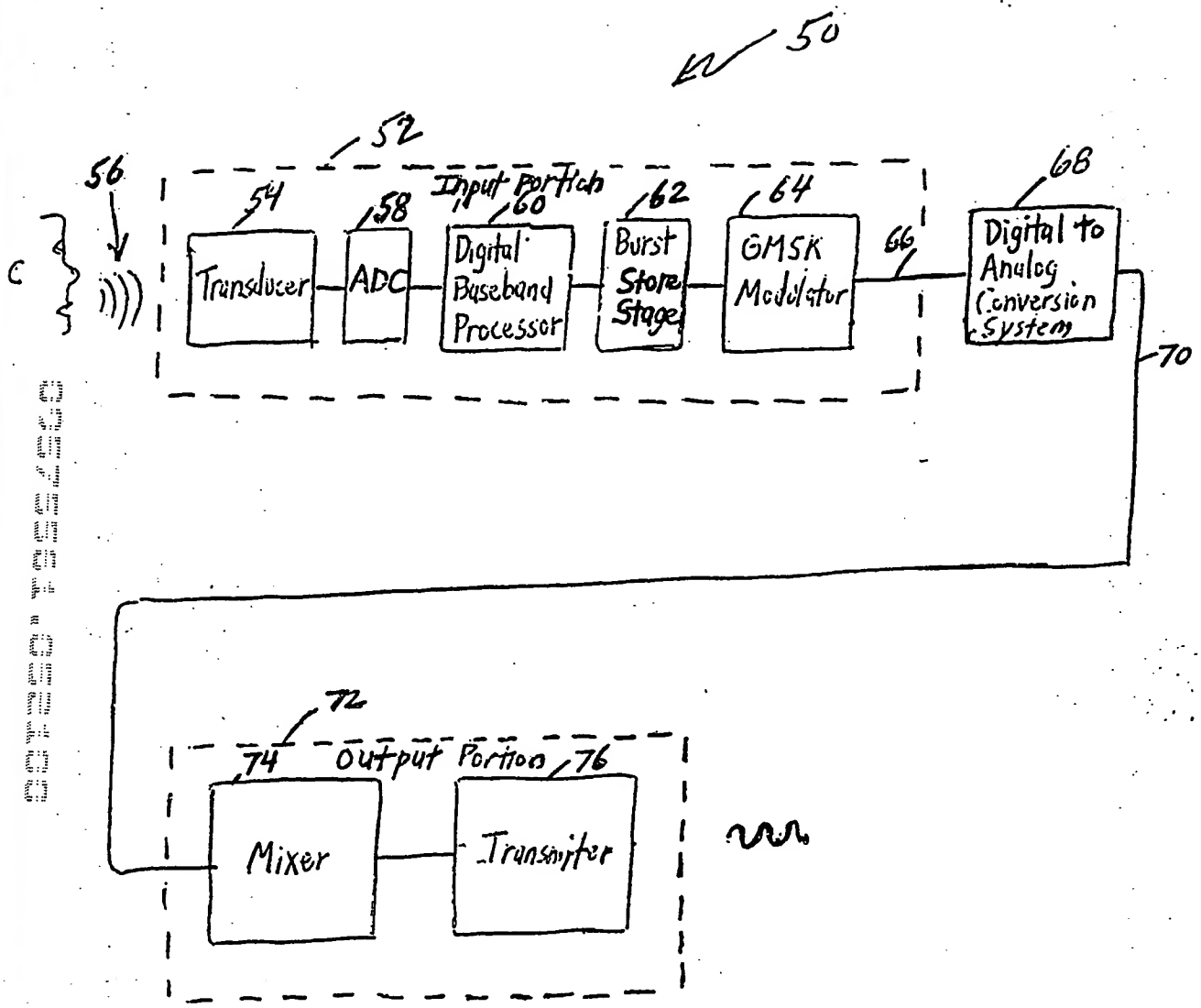

50
52
Input Portion
56
54
58
60
62
64
66
68
70
C
Transducer
ADC
Digital Baseband Processor
Burst Store Stage
GMSK Modulator
Digital to Analog Conversion System
72
74
Output Portion
76
Mixer
Transmitter

FIG. 1

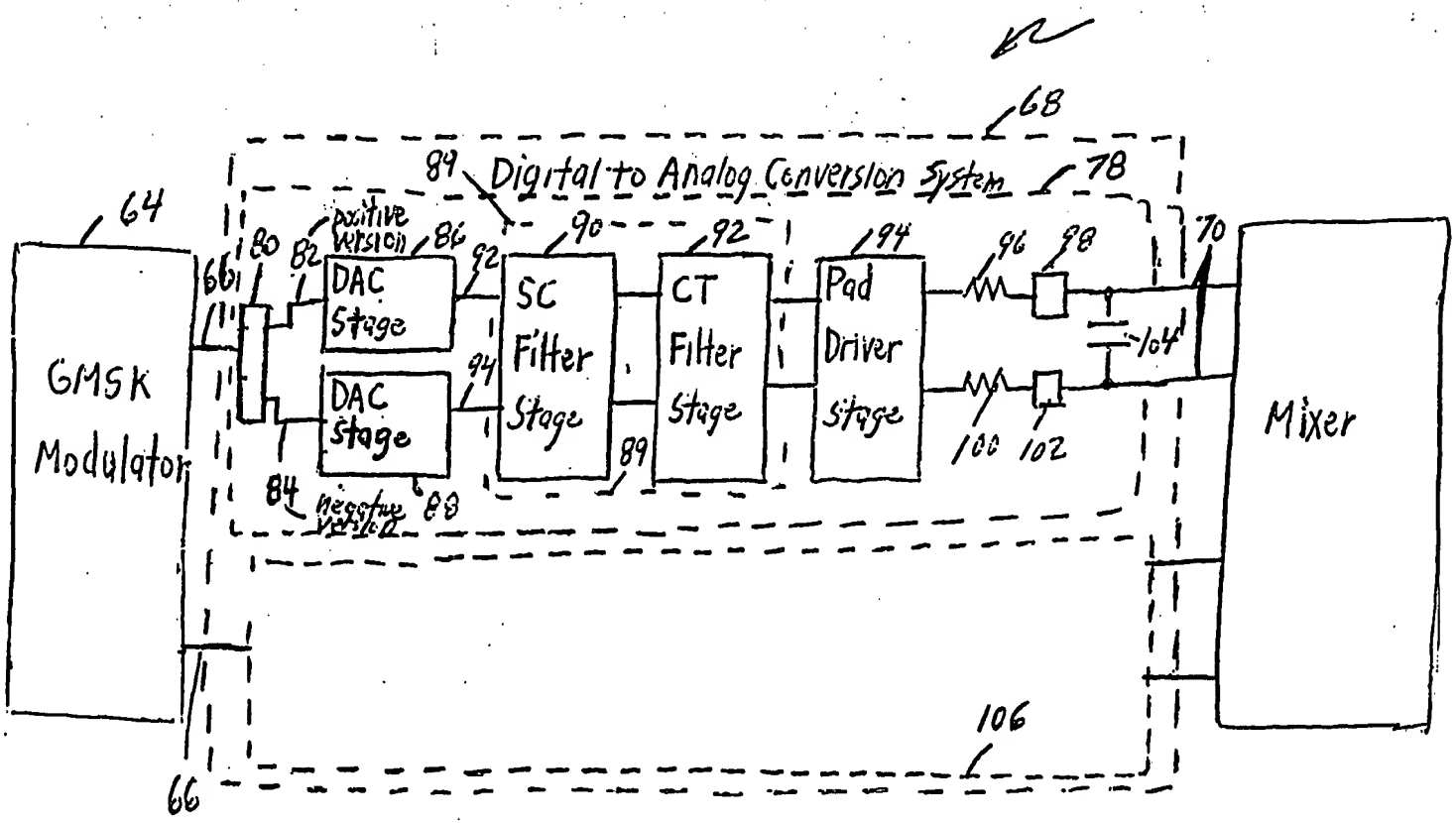

68
89
Digital to Analog Conversion System
78
64
positive version
80
82
86
92
90
92
94
96
98
70
66
DAC Stage
SC Filter Stage
CT Filter Stage
Pad Driver stage
104
GMSK Modulator
DAC Stage
94
89
100
102
Mixer
84
negative version
88
106
66

FIG. 2

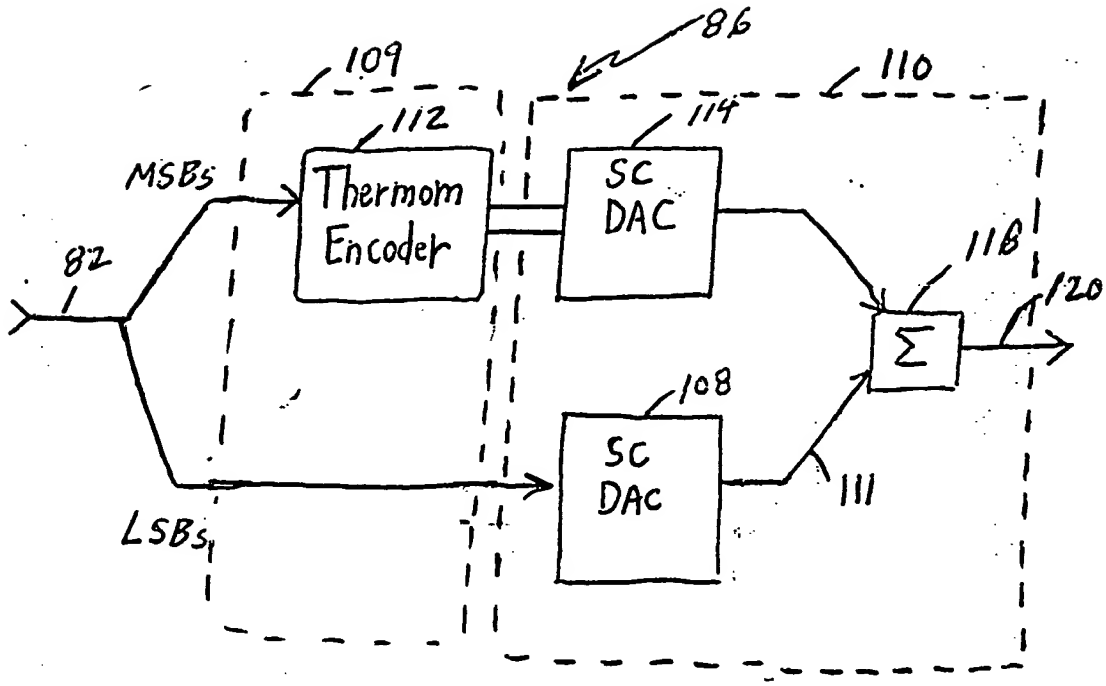

86
109
110
112
114
MSBs
Thermom Encoder
SC DAC
82
116
120
Σ
108
SC DAc
111
LSBs

FIG. 3

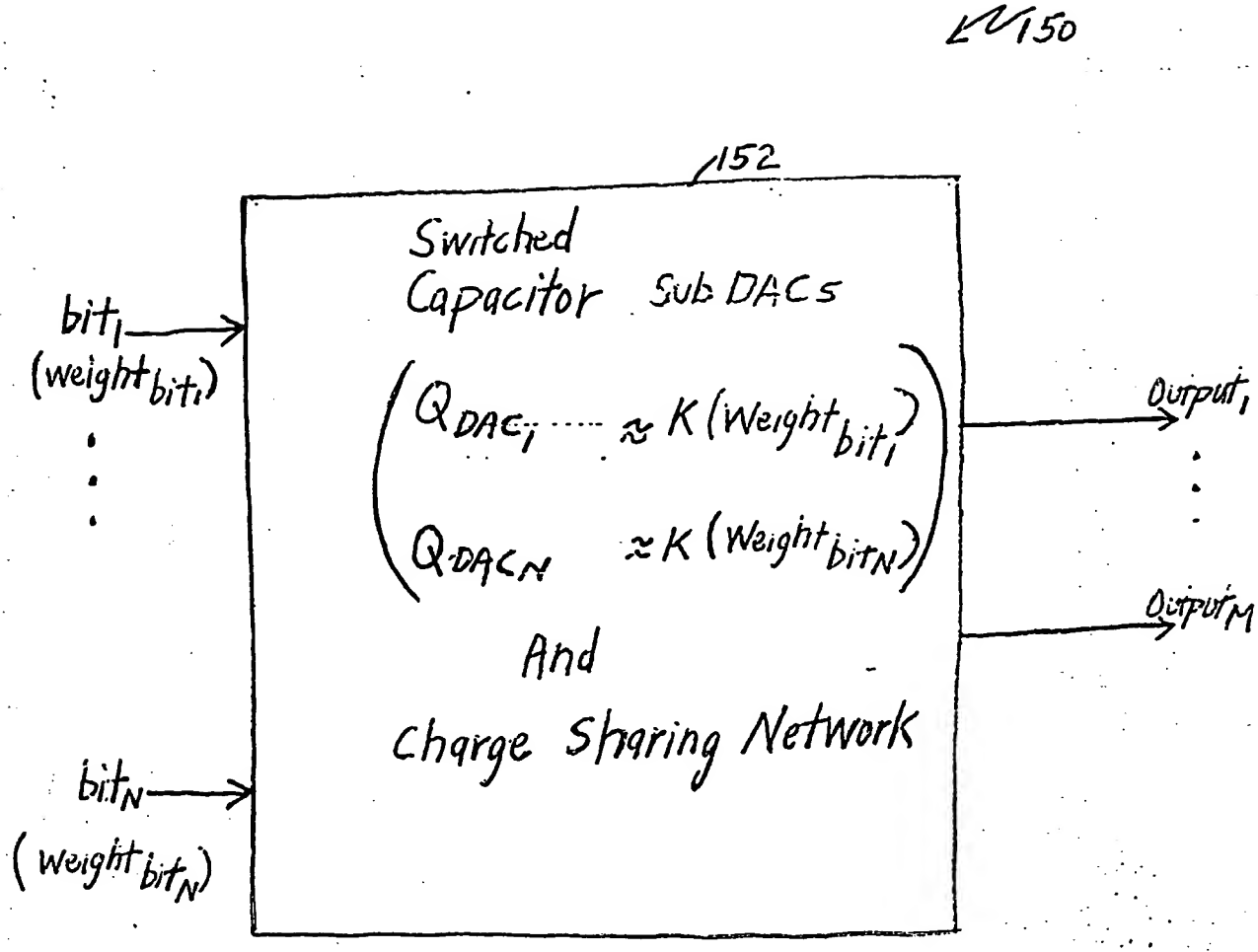

150
152
Switched
Capacitor Sub DACs
bit_1
$(weight_{bit_1})$
bit_N
$(weight_{bit_N})$
$Q_{DAC_1} \approx K(Weight_{bit_1})$
$Q_{DAC_N} \approx K(Weight_{bit_N})$
And
Charge Sharing Network
$Output_1$
$Output_M$

FIG. 4

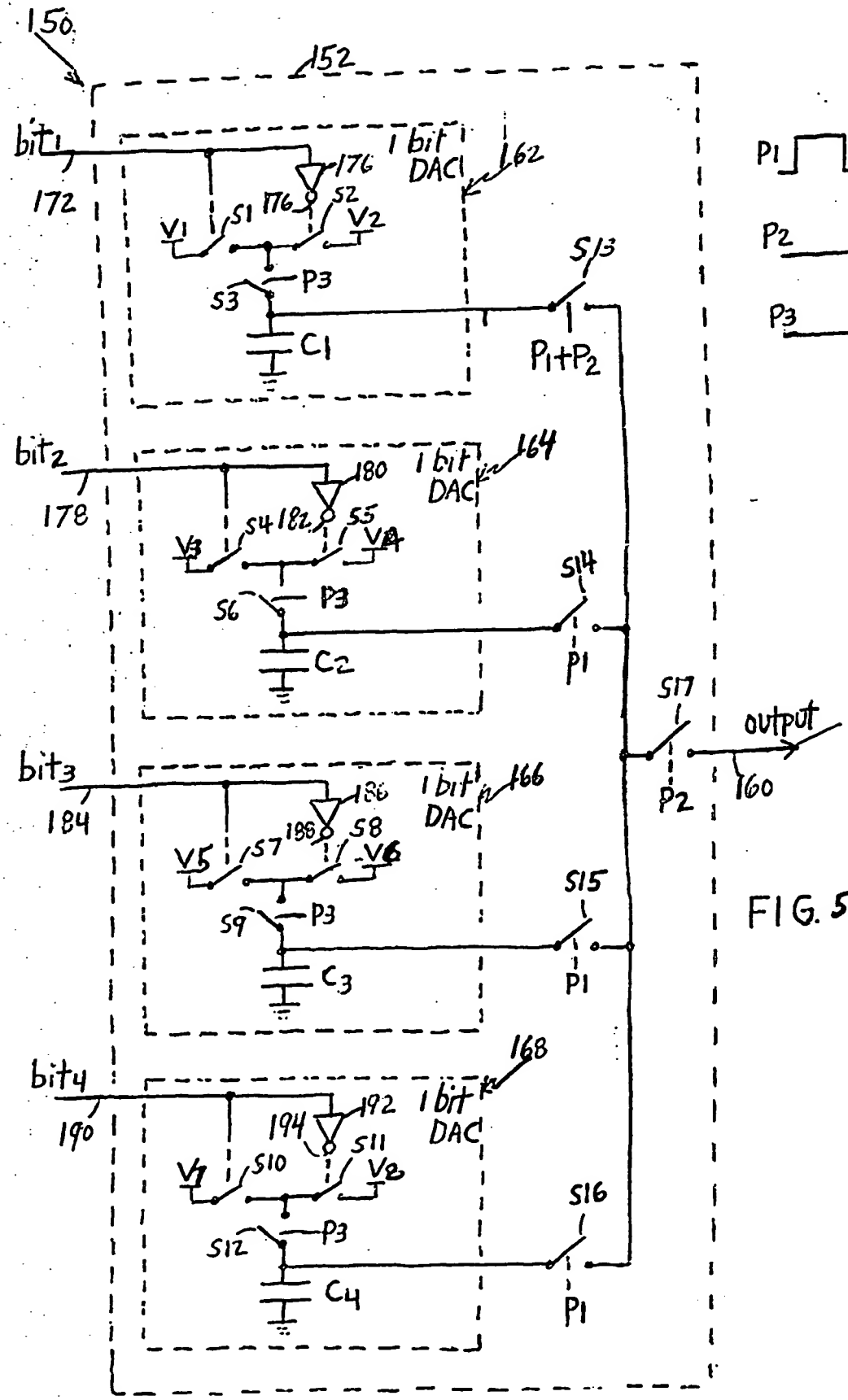

150
152
bit1
172
1 bit DAC
162
176
176
S1
S2
V1
V2
P3
S3
C1
S13
P1+P2
bit2
178
1 bit DAC
164
180
182
S4
S5
V3
V4
P3
S6
C2
S14
P1
S17
output
160
P2
bit3
184
1 bit DAC
166
186
188
S7
S8
V5
V6
P3
S9
C3
S15
P1
bit4
190
1 bit DAC
168
192
194
S10
S11
V7
V8
P3
S12
C4
S16
P1

FIG. 5

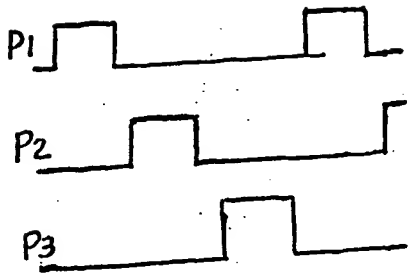

P1
P2
P3

FIG. 6

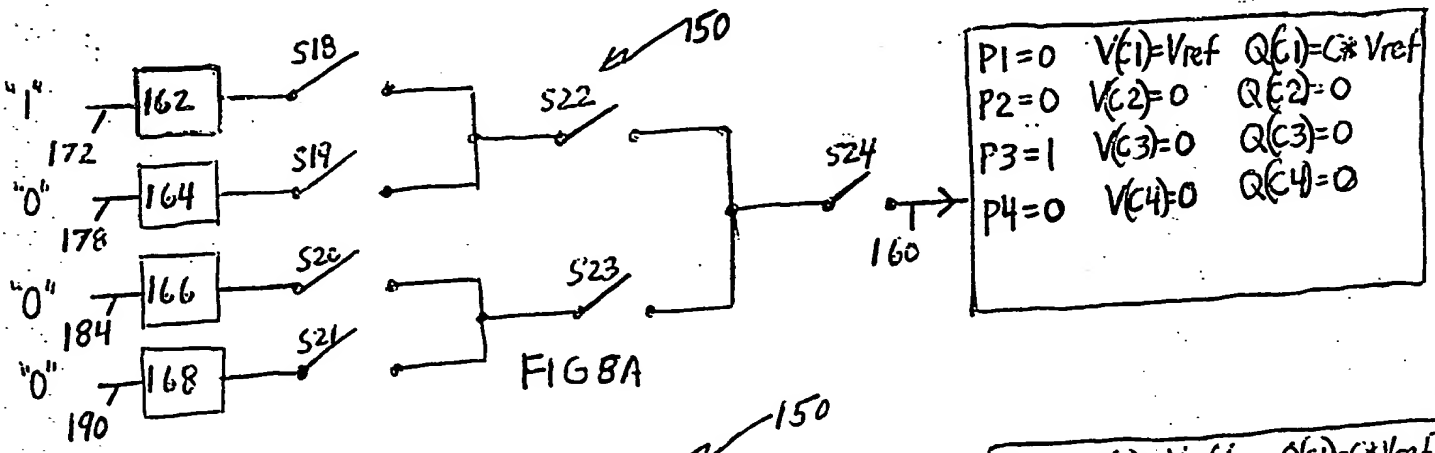


FIG 8A

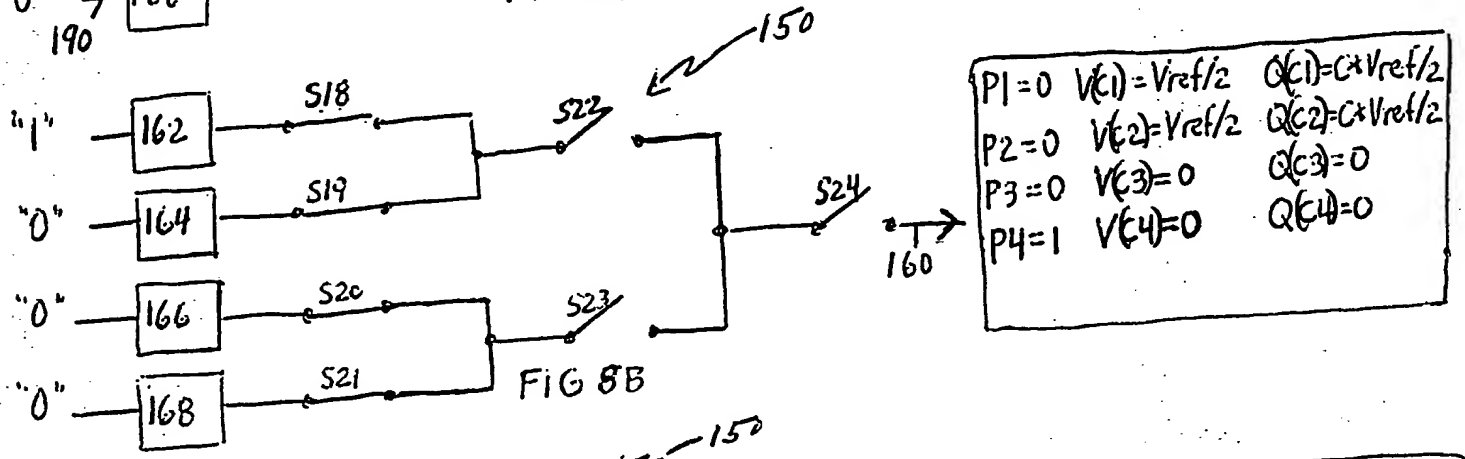


FIG 8B

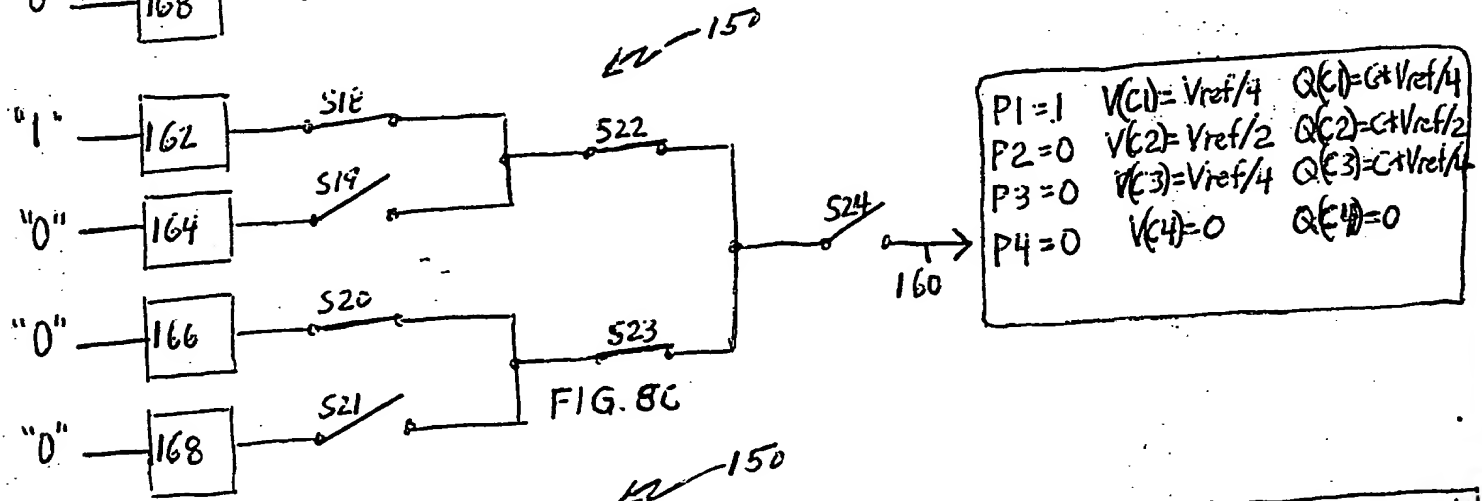


FIG. 8C

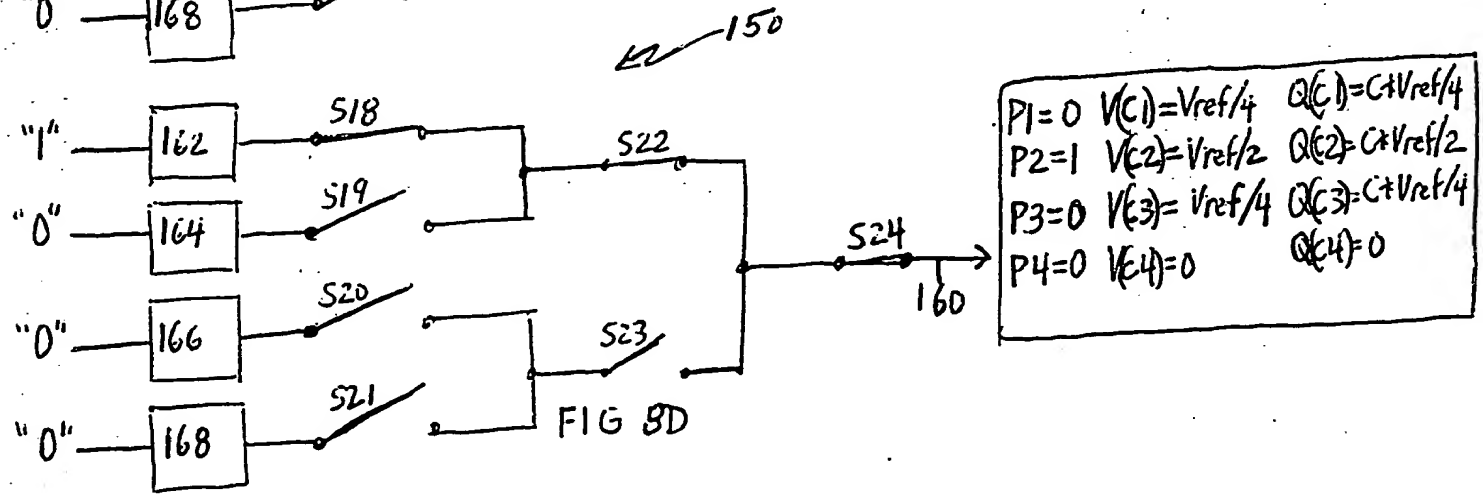


FIG 8D

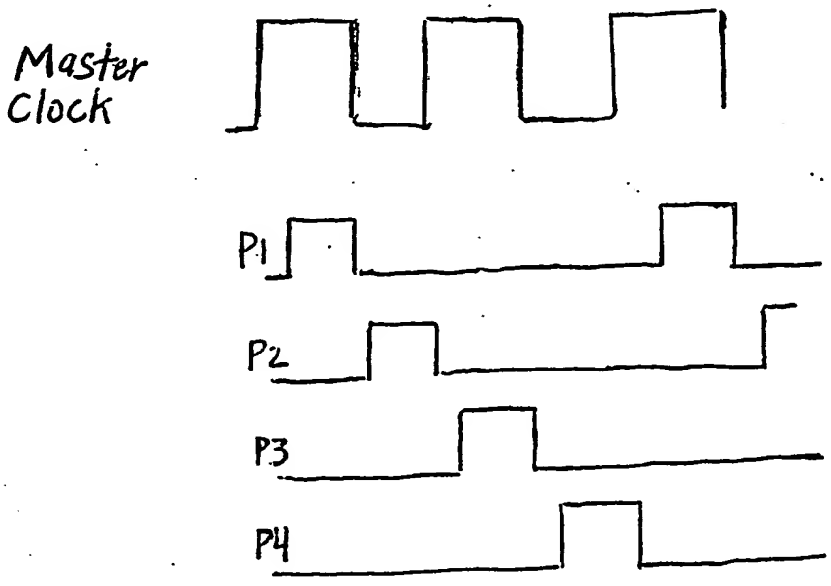


FIG 9

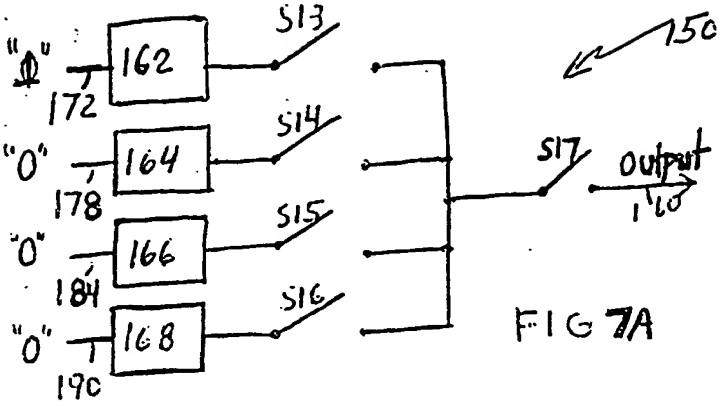


FIG 7A

P1 "0"	$V(C_1) = V_{ref}$	$Q(C_1) = C * V_{ref}$
P2 "0"	$V(C_2) = 0$	$Q(C_2) = 0$
P3 "1"	$V(C_3) = 0$	$Q(C_3) = 0$
	$V(C_4) = 0$	$Q(C_4) = 0$

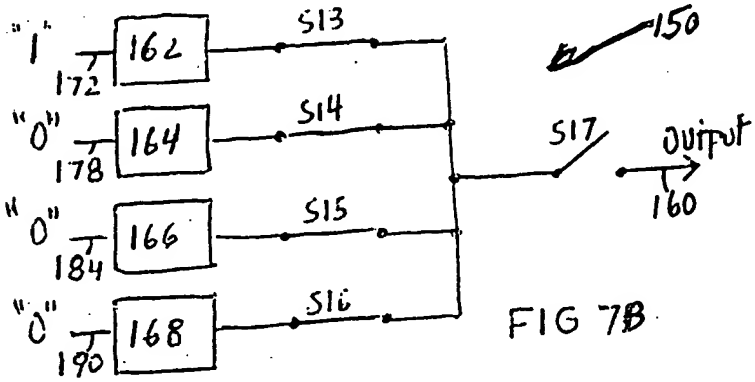


FIG 7B

P1 = "1"	$V(C1) = V_{ref}/4$	$Q(C1) = C * V_{ref}/4$
P2 = "0"	$V(C2) = V_{ref}/4$	$Q(C2) = C * V_{ref}/4$
P3 = "0"	$V(C3) = V_{ref}/4$	$Q(C3) = C * V_{ref}/4$
	$V(C4) = V_{ref}/4$	$Q(C4) = C * V_{ref}/4$

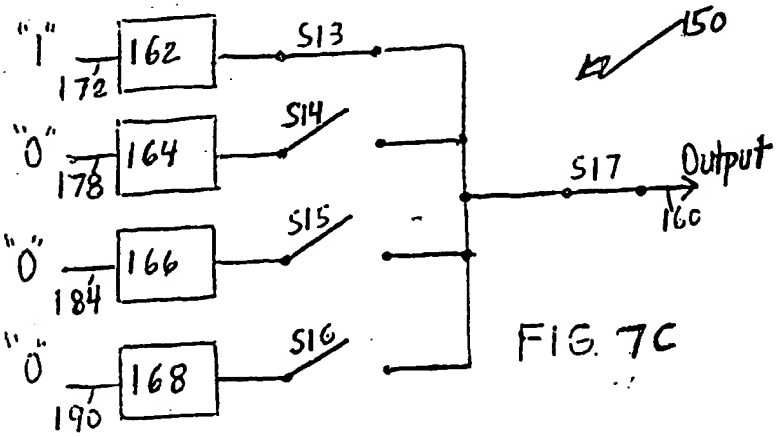


FIG. 7C

P1 = "0"	$V(C1) = V_{ref}/4$	$Q(C1) = C * V_{ref}/4$
P2 = "1"	$V(C2) = V_{ref}/4$	$Q(C2) = C * V_{ref}/4$
P3 = "0"	$V(C3) = V_{ref}/4$	$Q(C3) = C * V_{ref}/4$
	$V(C4) = V_{ref}/4$	$Q(C4) = C * V_{ref}/4$

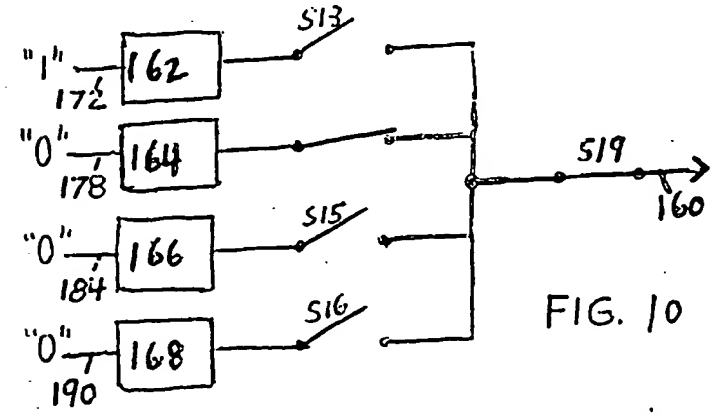


FIG. 10

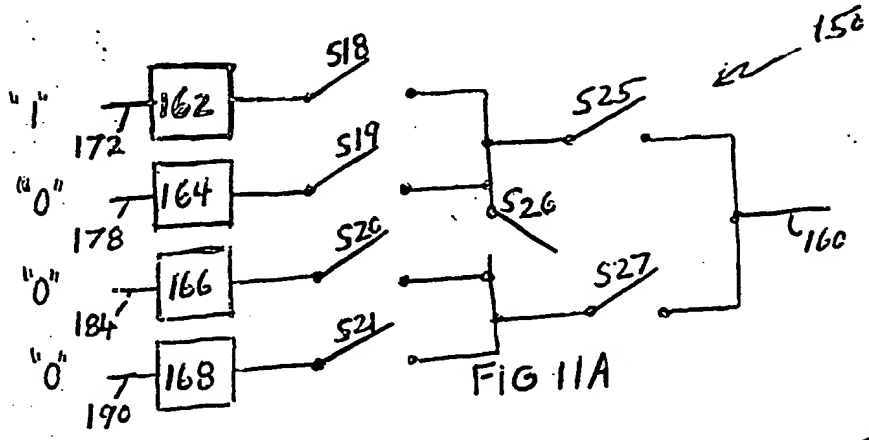


FIG 11A

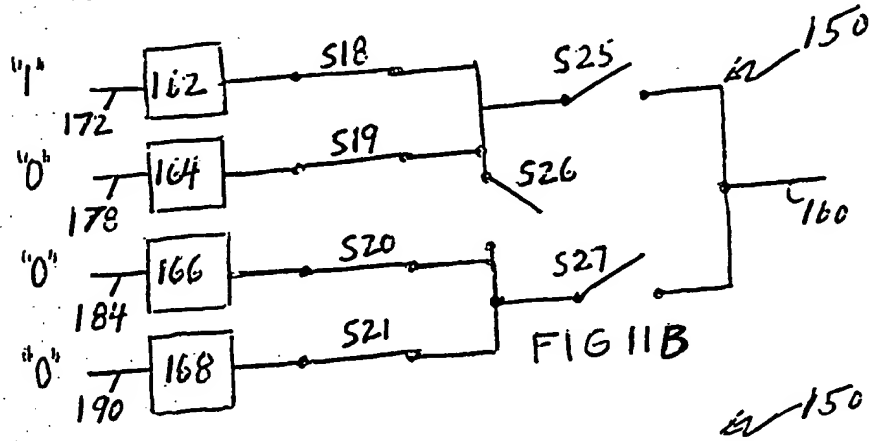


FIG 11B

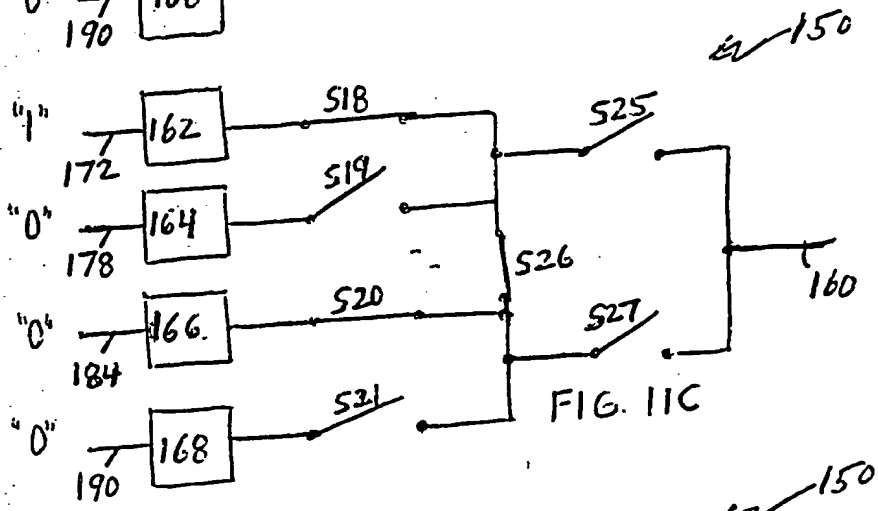


FIG. 11C

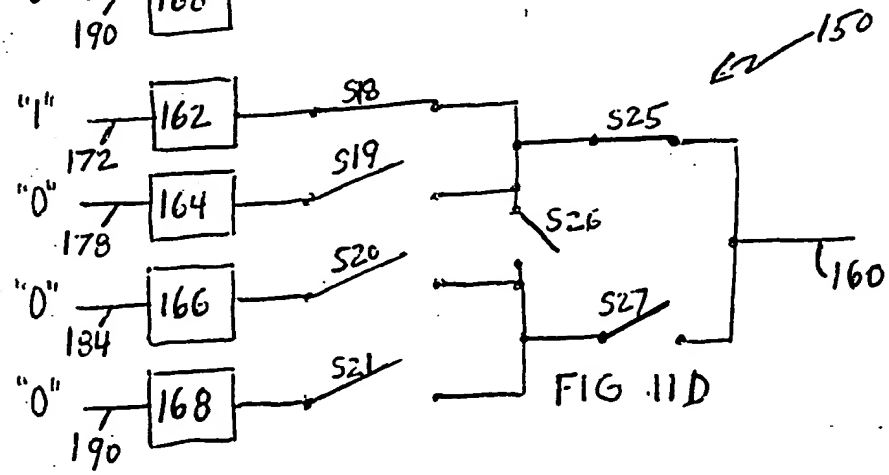


FIG 11D

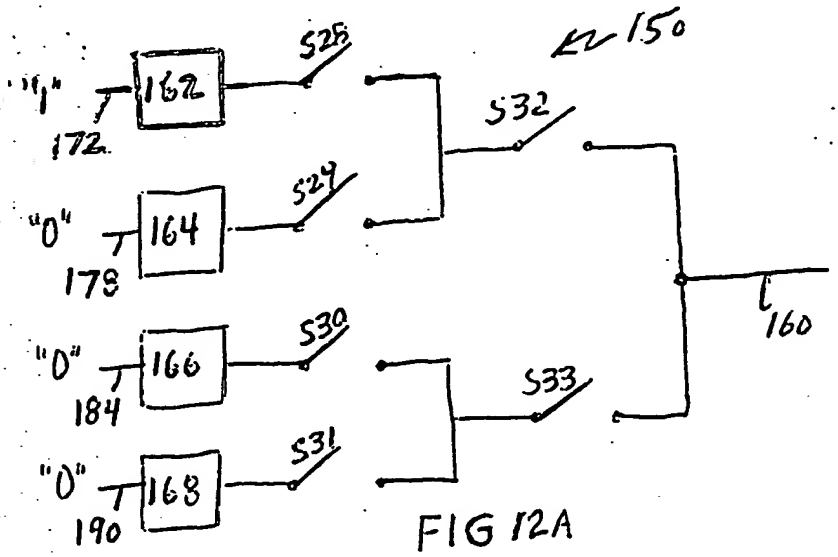


FIG 12A

P1 = 0 V(C1) = Vref Q(C1) = C * Vref
P2 = 0 V(C2) = 0 Q(C2) = 0
P3 = 1 V(C3) = 0 Q(C3) = 0
V(C4) = 0 Q(C4) = 0

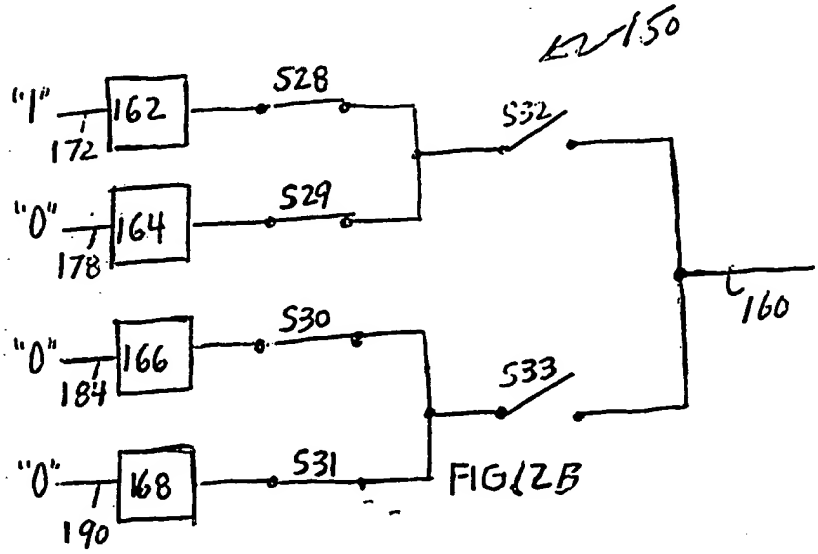


FIG 12B

P1 = 1 V(C1) = Vref/2 Q(C1) = C * Vref/2
P2 = 0 V(C2) = Vref/2 Q(C2) = C * Vref/2
P3 = 0 V(C3) = 0 Q(C3) = 0
V(C4) = 0 Q(C4) = 0

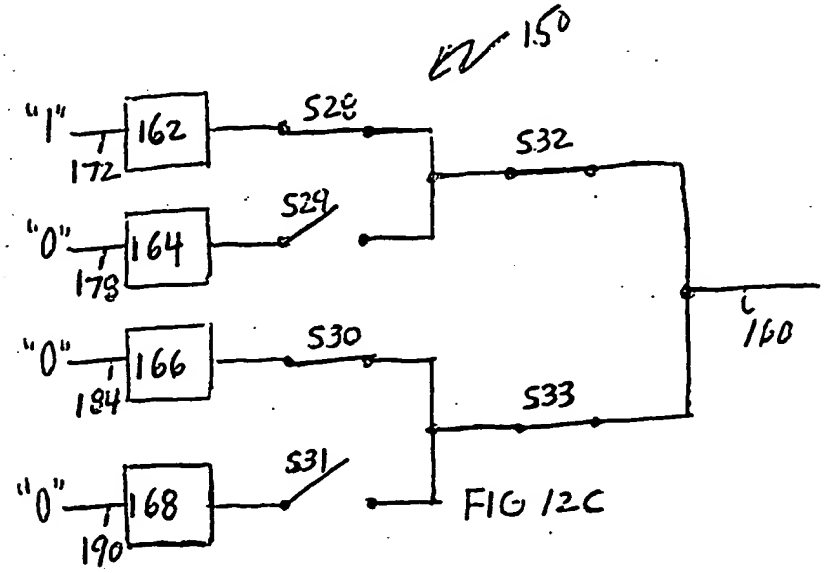


FIG 12C

P1 = 0 V(C1) = Vref/2 Q(C1) = C * Vref/2
P2 = 1 V(C2) = Vref/2 Q(C2) = C * Vref/2
P3 = 0 V(C3) = 0 Q(C3) = 0
V(C4) = 0 Q(C4) = 0

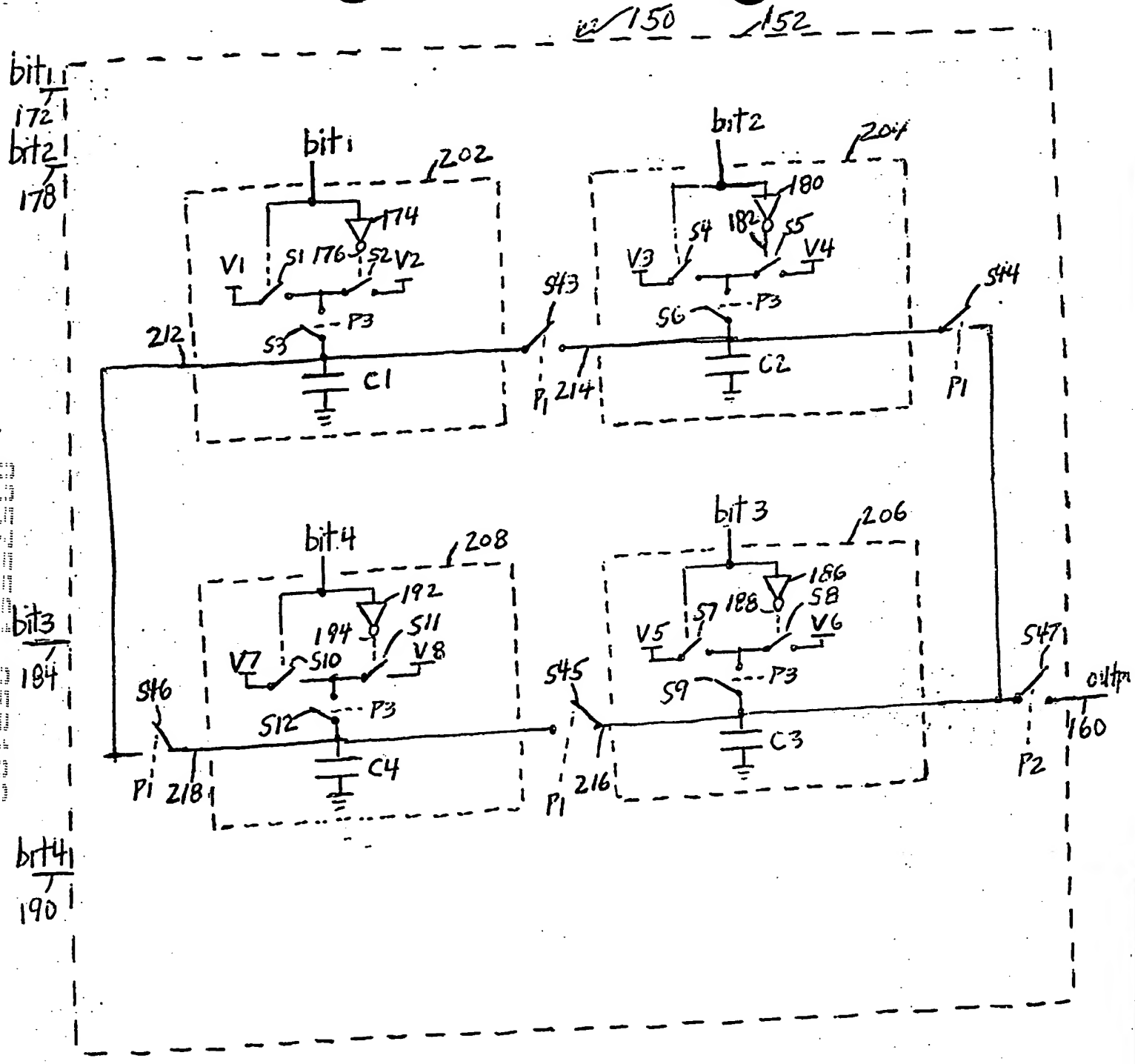
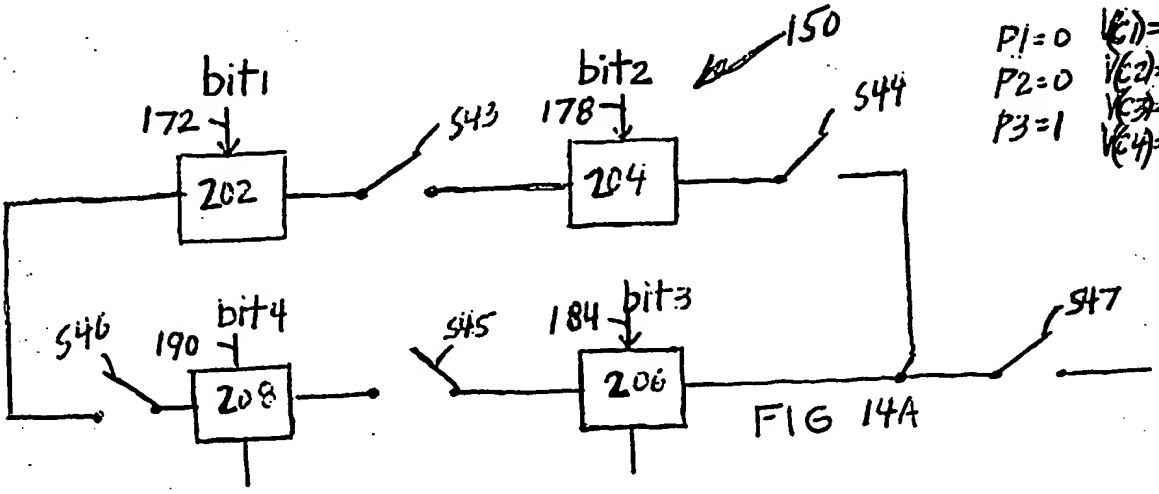
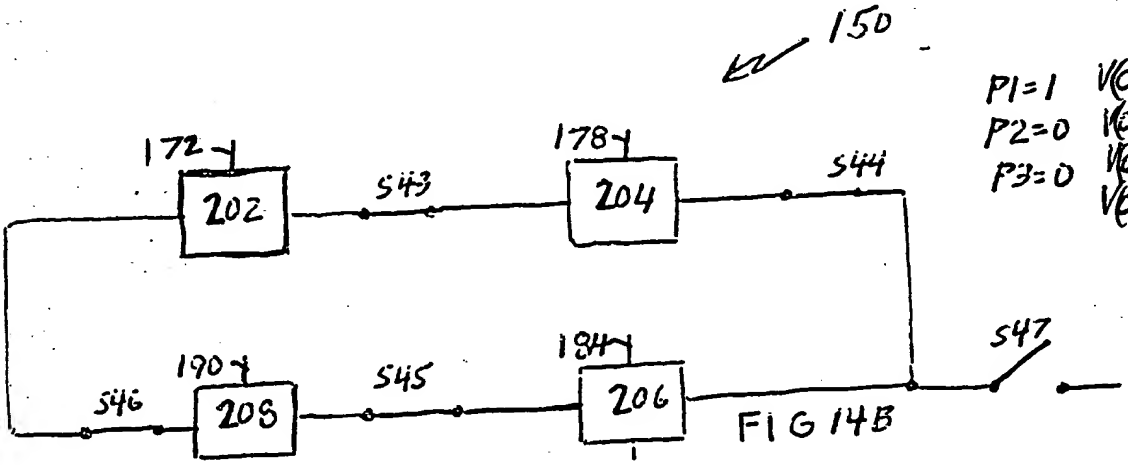

150
152
bit1
172
bit2
178
bit3
184
bit4
190
bit1
202
bit2
204
bit3
206
bit4
208
174
176
180
182
186
188
192
194
V1
S1
S2
V2
V3
S4
S5
V4
V5
S7
S8
V6
V7
S10
S11
V8
S3
S6
S9
S12
P3
C1
C2
C3
C4
212
214
216
218
P1
P2
S43
S44
S45
S46
S47
output
160

FIG. 13



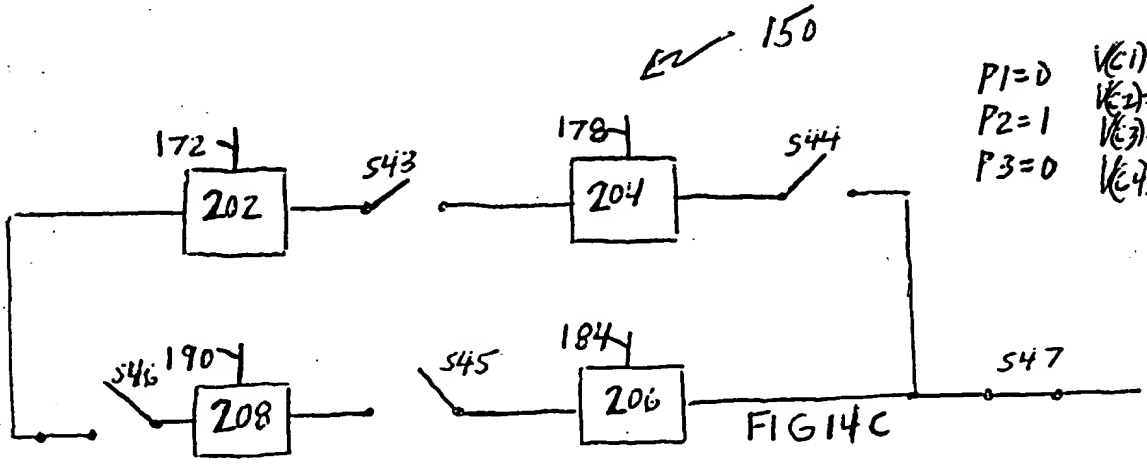
P1=0 V(C1)=Vref Q(C1)=C*Vref
P2=0 V(C2)=0 Q(C2)=0
P3=1 V(C3)=0 Q(C3)=0
V(C4)=0 Q(C4)=0

FIG 14A



P1=1 V(C1)=Vref/4 Q(C1)=C*Vref/4
P2=0 V(C2)=Vref/4 Q(C2)=C*Vref/4
P3=0 V(C3)=Vref/4 Q(C3)=C*Vref/4
V(C4)=Vref/4 Q(C4)=C*Vref/4

FIG 14B



P1=0 V(C1)=Vref/4 Q(C1)=C*Vref/4
P2=1 V(C2)=Vref/4 Q(C2)=C*Vref/4
P3=0 V(C3)=Vref/4 Q(C3)=C*Vref/4
V(C4)=Vref/4 Q(C4)=C*Vref/4

FIG 14C

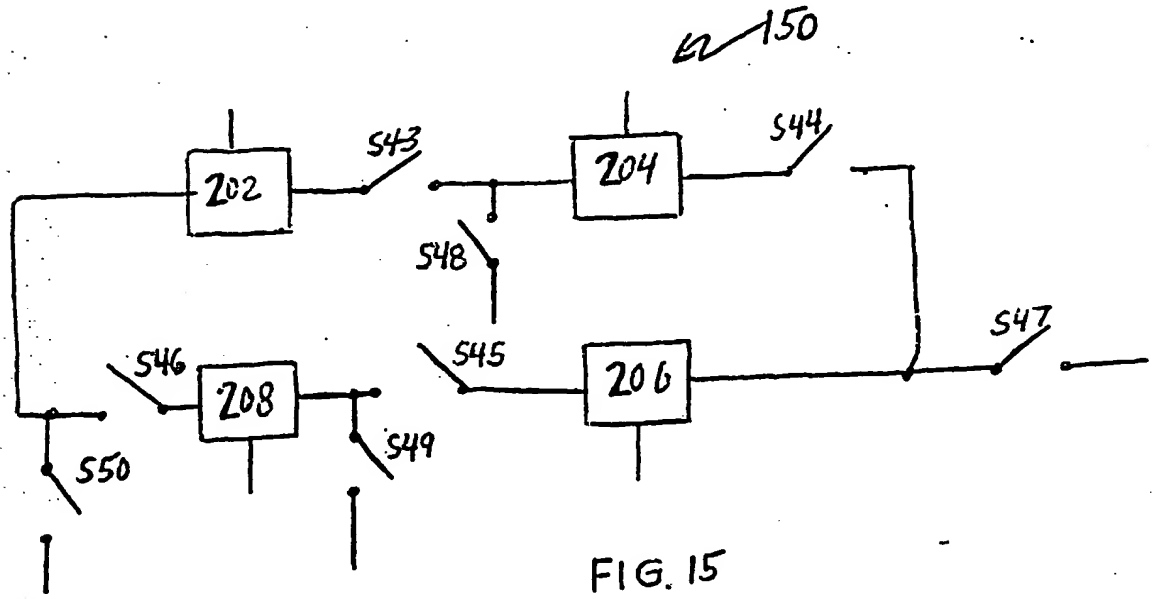


FIG. 15

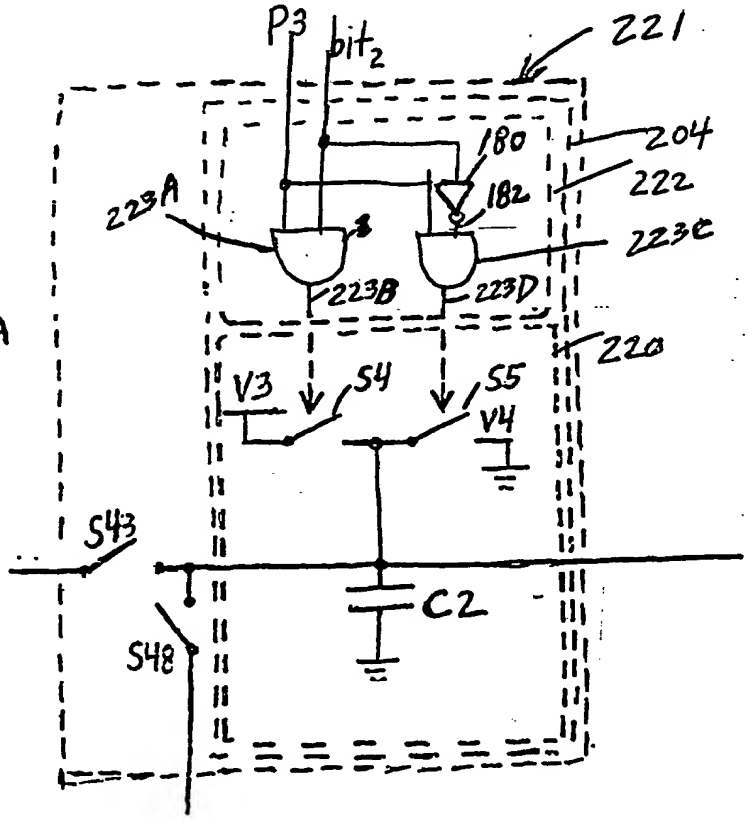


FIG 16A

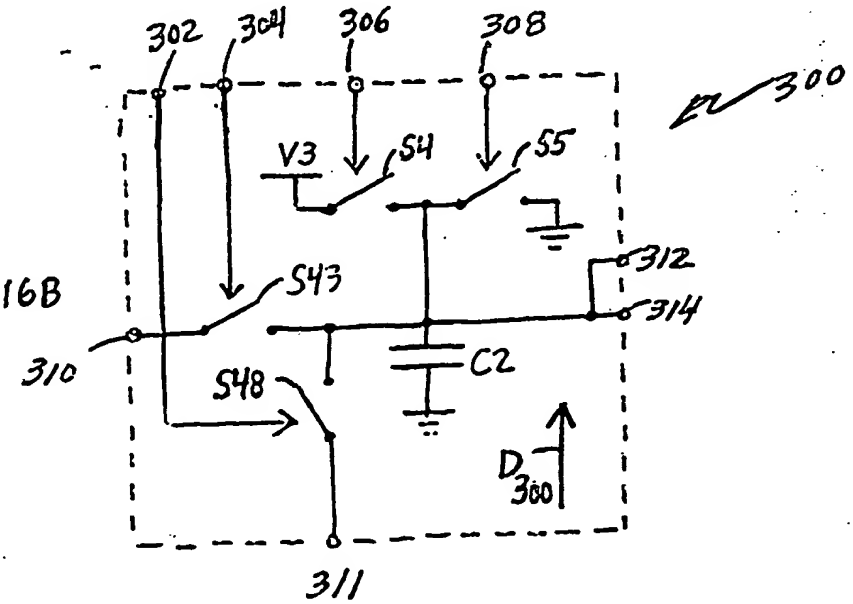


FIG 16B

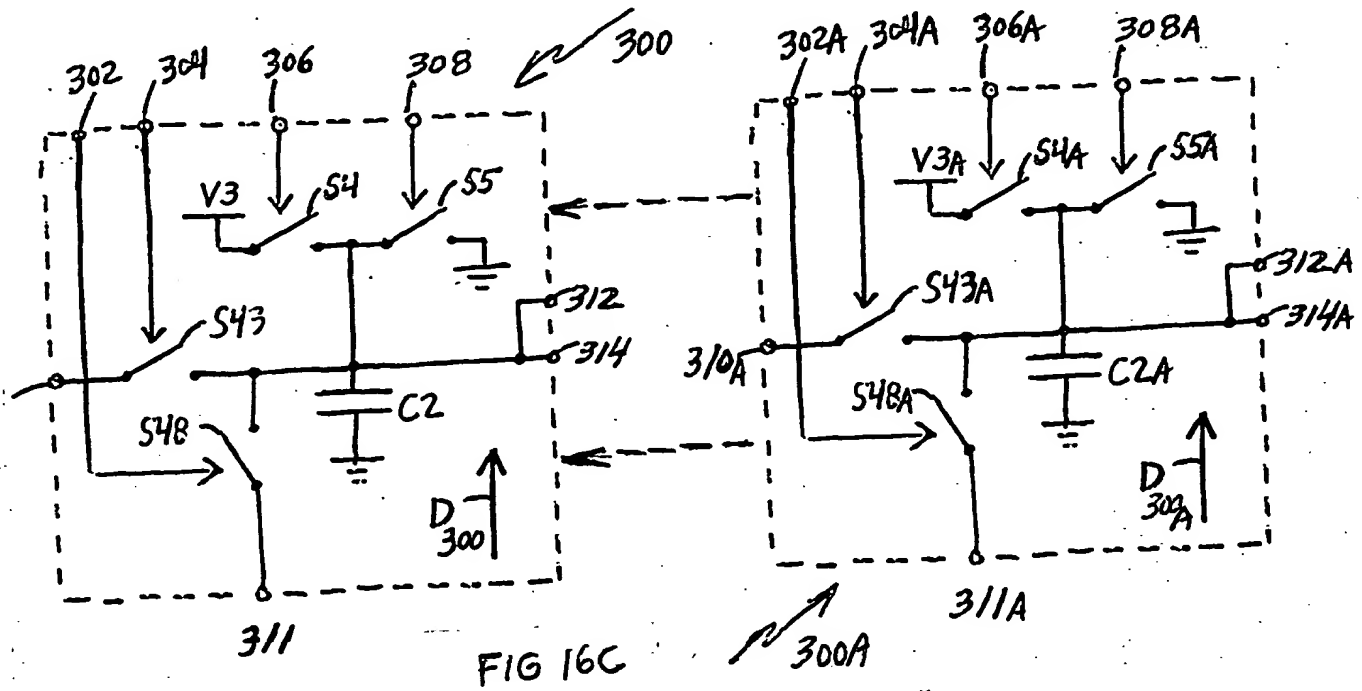


FIG 16C

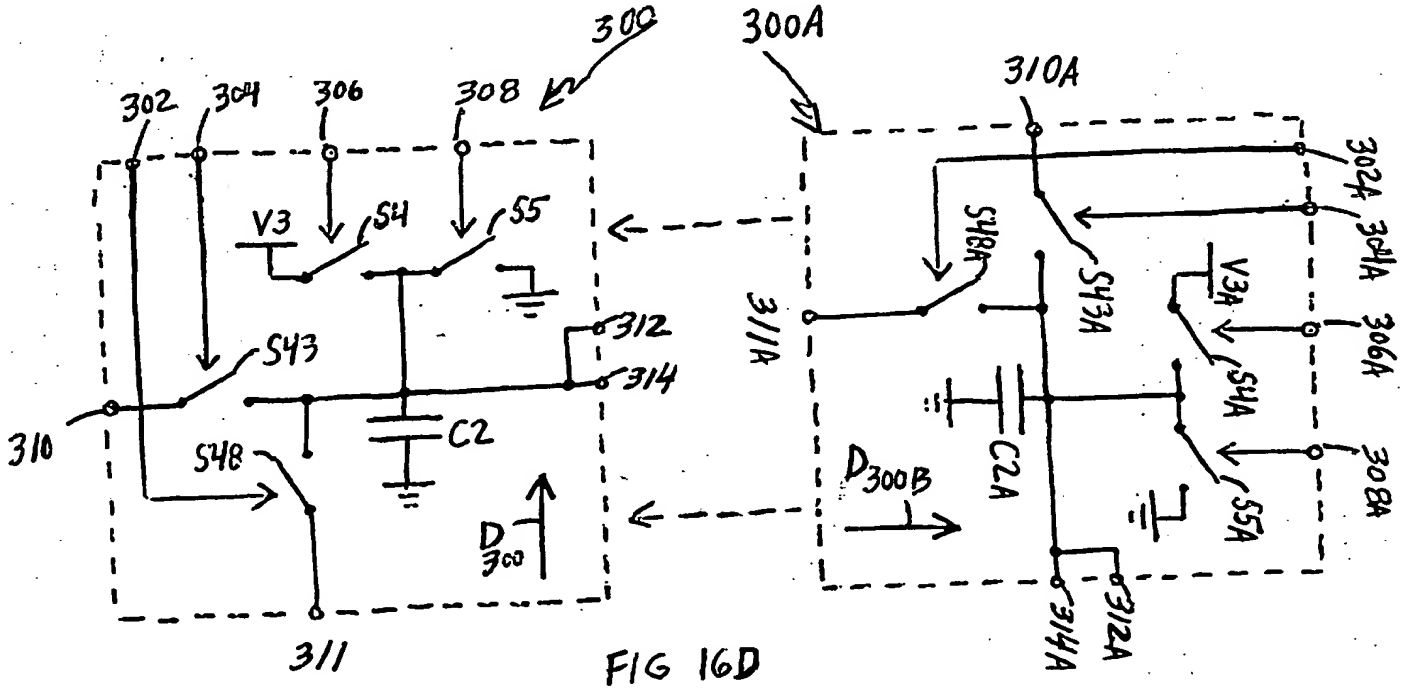
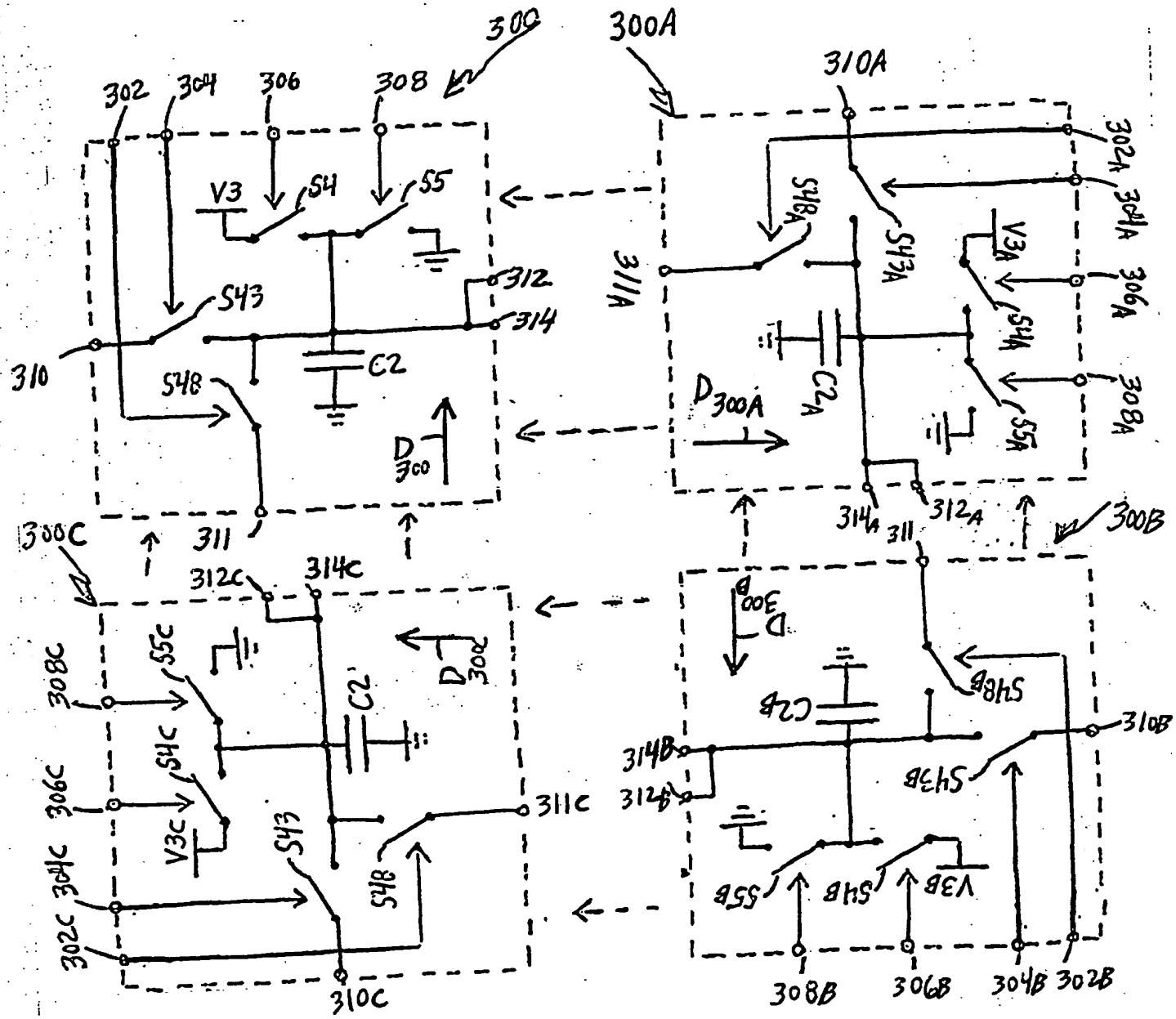


FIG 16D


300
300A
300B
300C
302
304
306
308
310
311
312
314
V3
S4
S5
S43
S48
C2
D300
302A
304A
306A
308A
310A
311A
312A
314A
V3A
S4A
S5A
S43A
S48A
C2A
D300A
302B
304B
306B
308B
310B
311B
312B
314B
V3B
S4B
S5B
S43B
S48B
C2B
D300B
302C
304C
306C
308C
310C
311C
312C
314C
V3C
S4C
S5C
S43C
S48C
C2C
D300C

16E

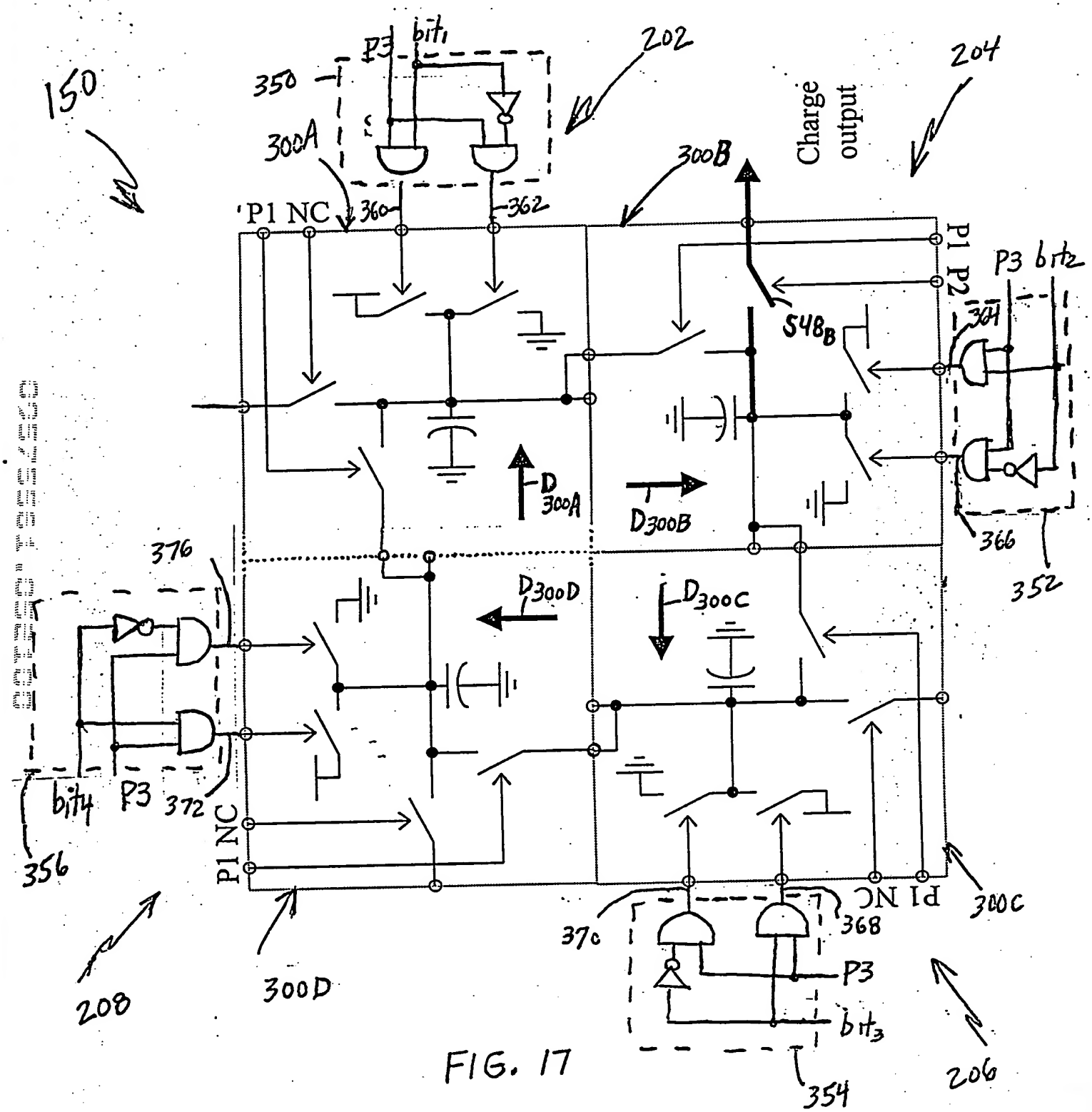

150
202
204
350
300A
300B
bit1
P3
Charge output
P1 NC
360
362
P1 P2
P3 bit2
361
S48B
D300A
D300B
D300C
D300D
366
352
376
bit4
P3
372
356
P1 NC
208
300D
370
368
P3
bit3
354
206
300C

FIG. 17

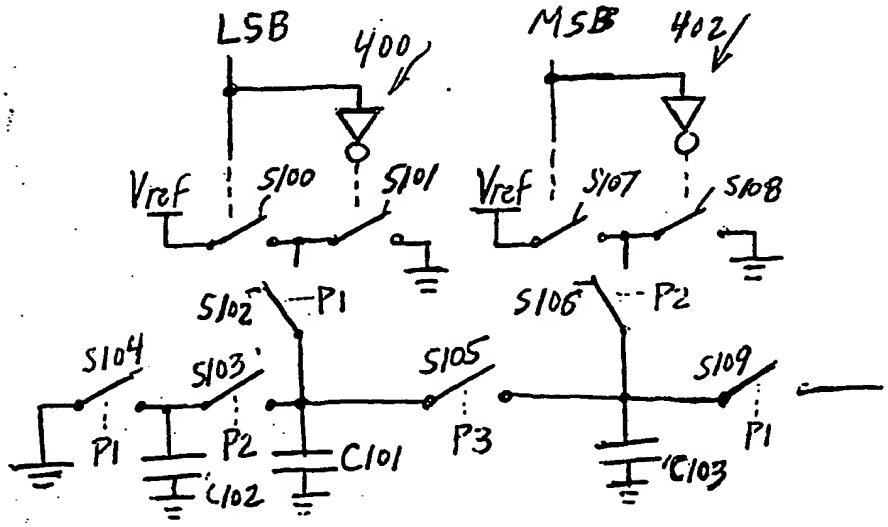

LSB
400
MSB
402
108
Vref
S100
S101
Vref
S107
S108
S102
P1
S106
P2
S104
S103
S105
S109
P1
P2
P3
P1
C101
C102
C103

FIG. 18

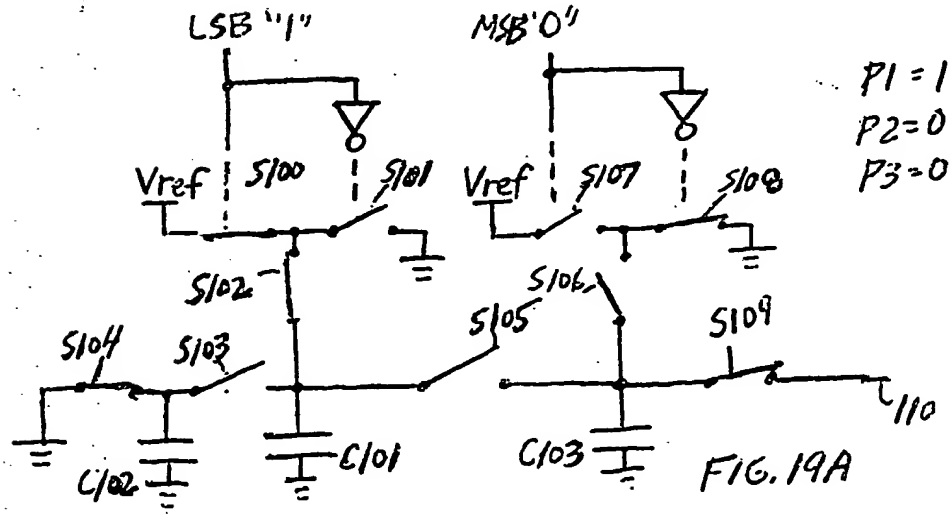


FIG. 19A

P1 = 1 V(C102) = 0 Q(C102) = 0
P2 = 0 V(C101) = Vref Q(C101) = C*Vref
P3 = 0 V(C103) = ? Q(C103) = ?

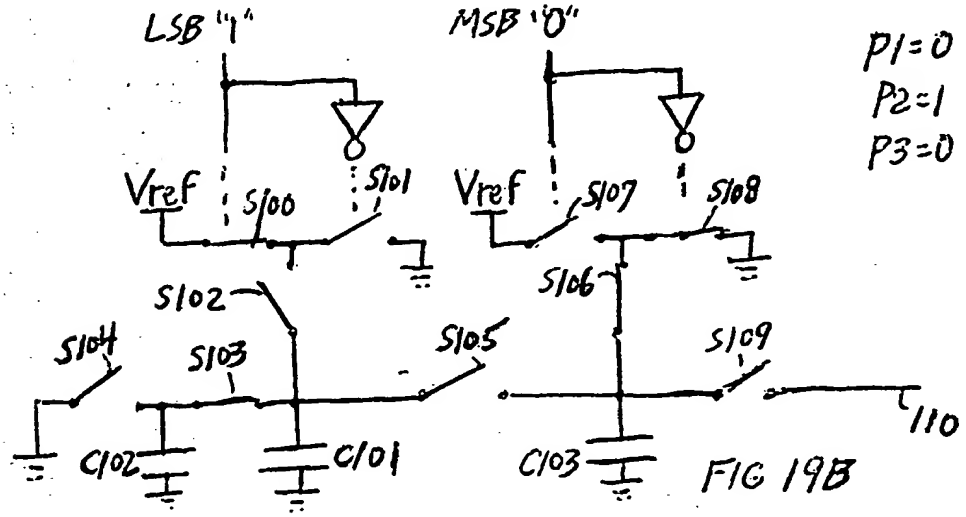


FIG 19B

P1 = 0 V(C102) = Vref/2 Q(C102) = C*Vref/2
P2 = 1 V(C101) = Vref/2 Q(C101) = C*Vref/2
P3 = 0 V(C103) = 0 Q(C103) = 0

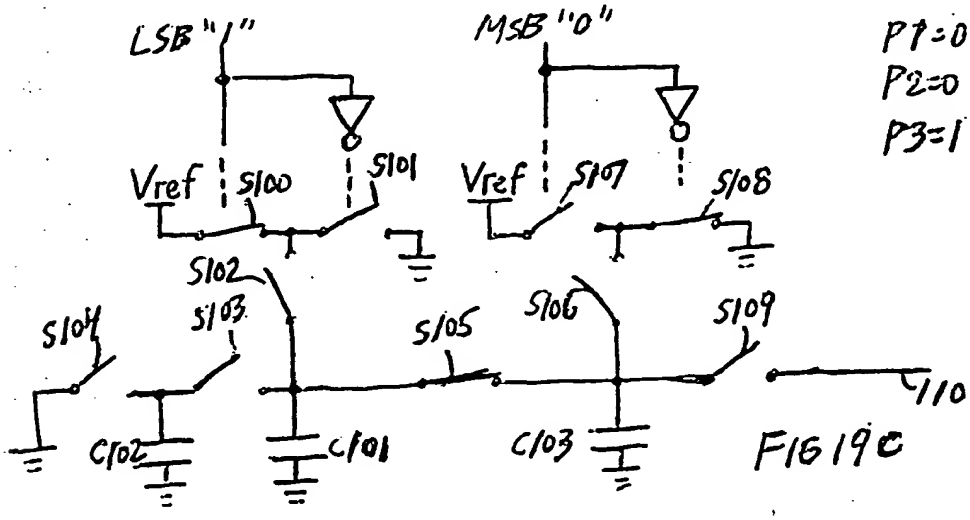


FIG 19C

P1 = 0 V(C102) = Vref/2 Q(C102) = C*Vref/2
P2 = 0 V(C101) = Vref/4 Q(C101) = C*Vref/4
P3 = 1 V(C103) = Vref/4 Q(C103) = C*Vref/4

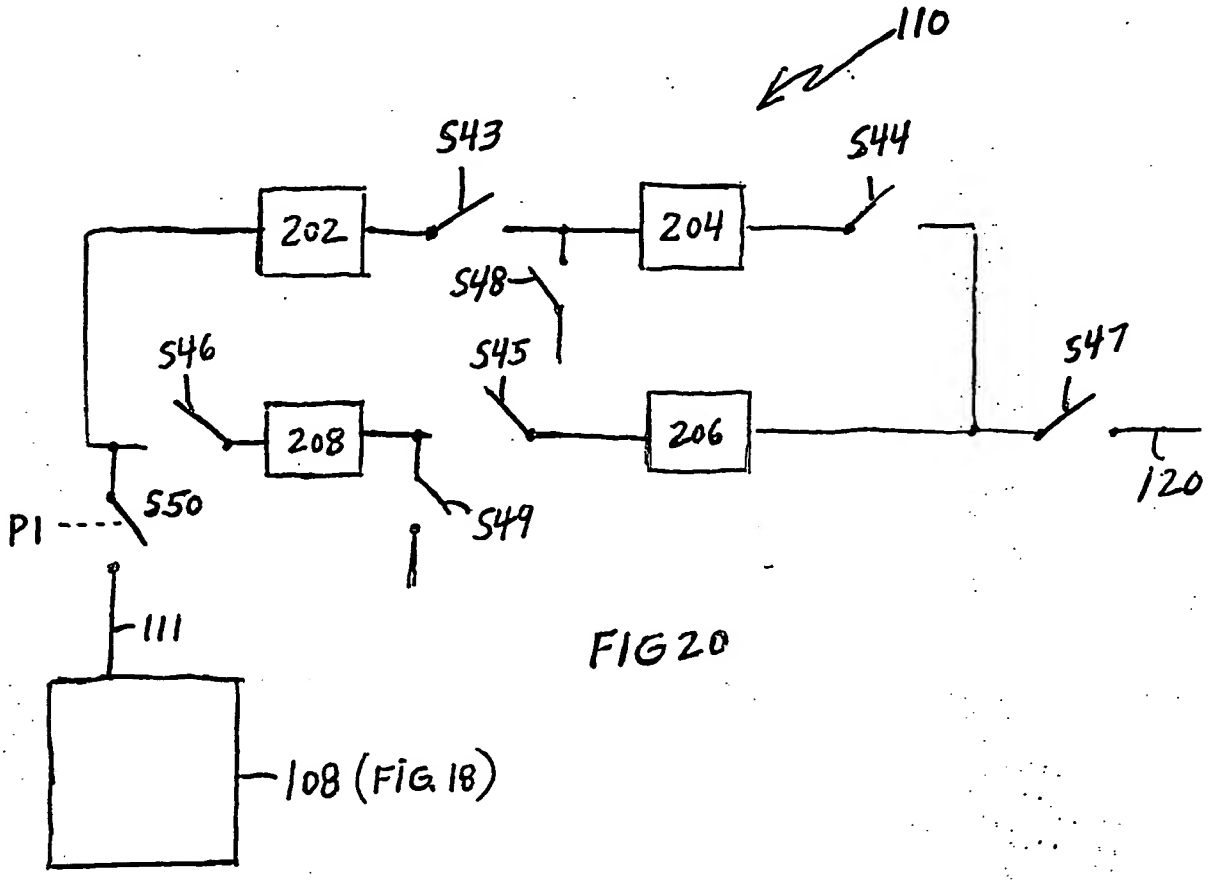
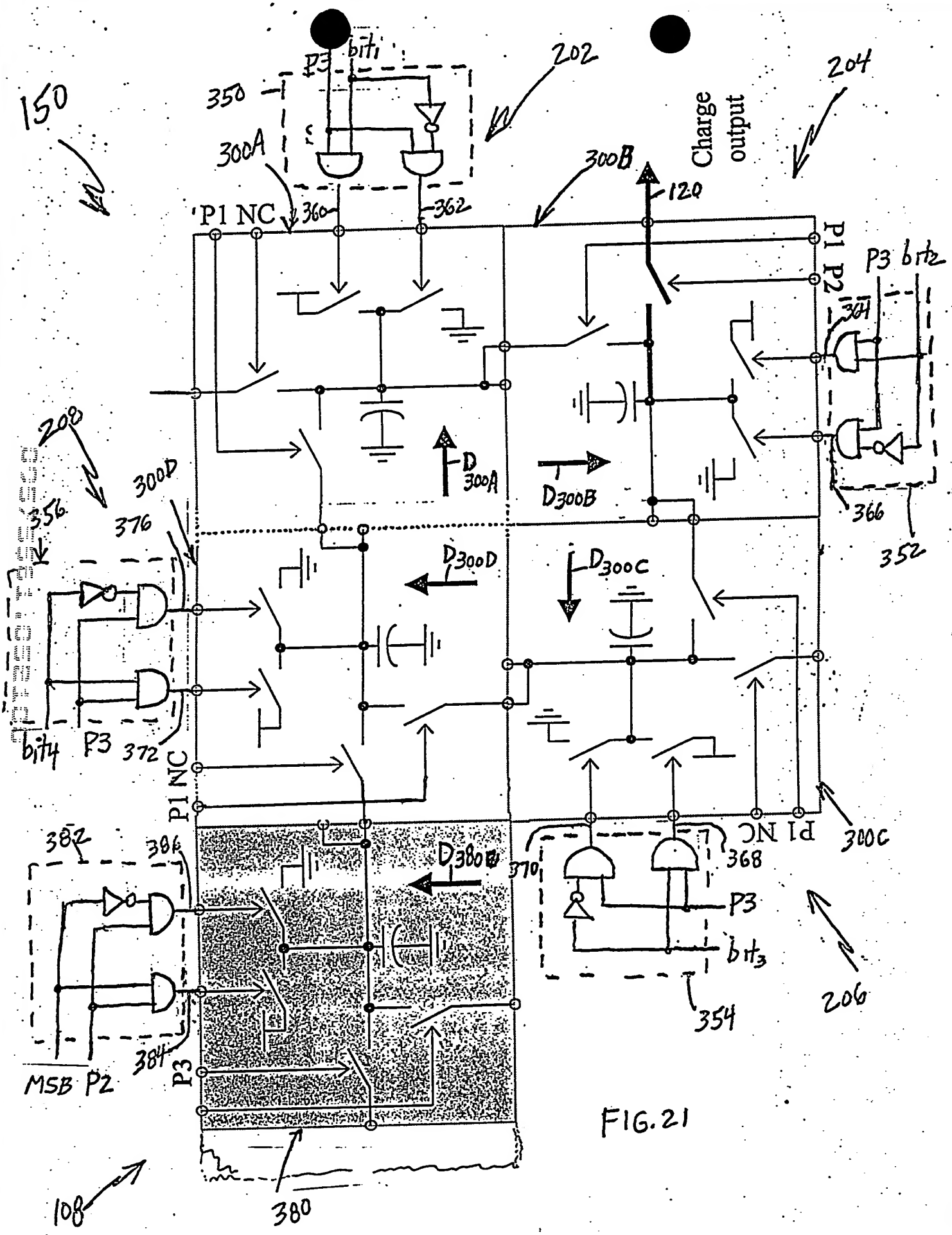

110
543
544
202
204
548
546
545
547
208
206
120
550
P1
549
111
108 (FIG 18)

FIG 20


150
202
204
350
300A
300B
Charge output
120
P1 NC
360
362
P1 P2
P3 bit2
364
208
300D
376
356
D300A
D300B
366
352
D300D
D300C
bit4
P3
372
P1 NC
382
386
D380
370
368
P3
bit3
354
206
300C
MSB P2
384
P3
108
380
FIG. 21

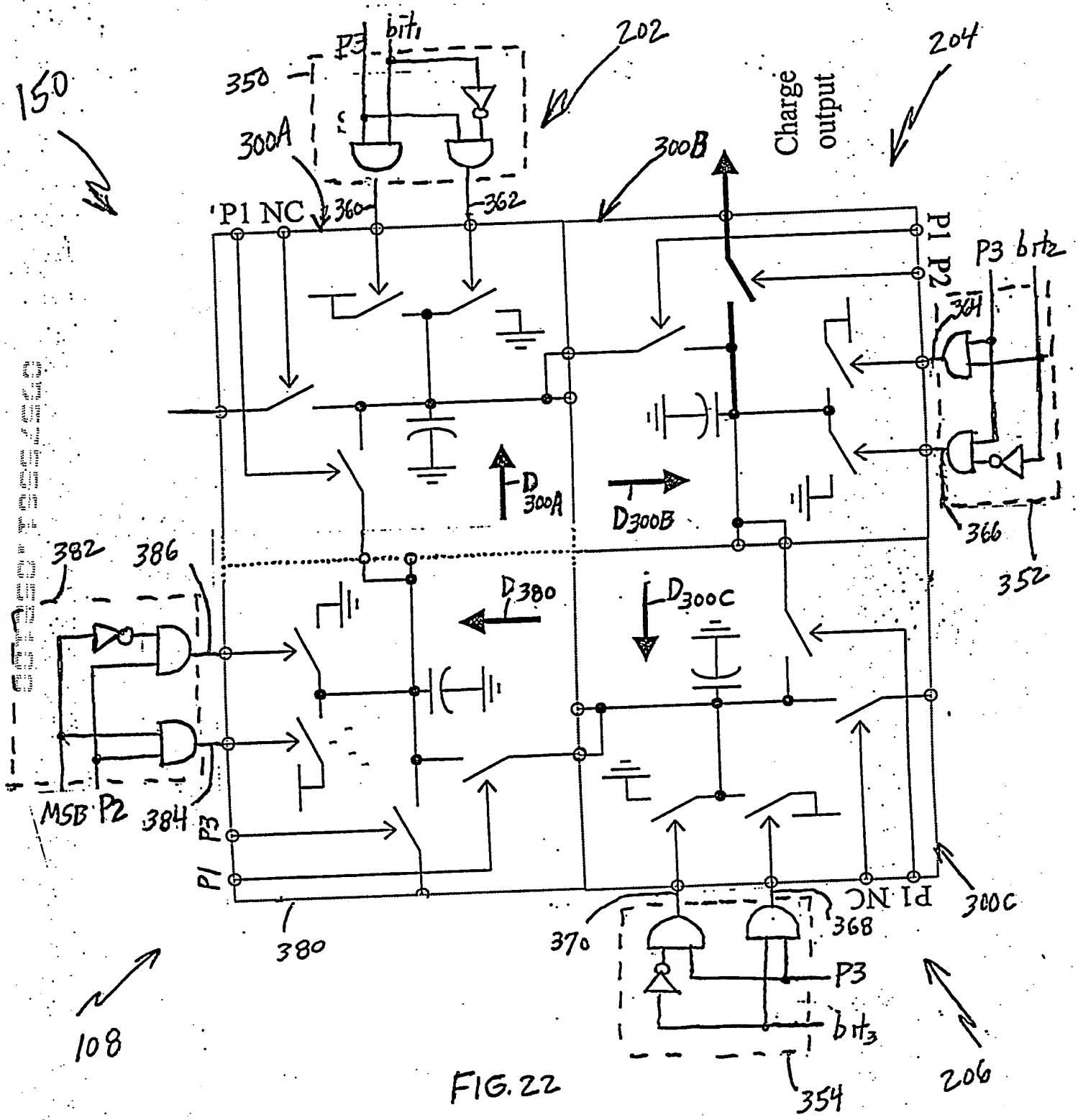

150
202
204
350
P3
bit1
300A
300B
Charge output
P1 NC
360
362
P1 P2
P3 bit2
364
366
352
D300A
D300B
382
386
D380
D300C
MSB P2
384
P1 P3
380
370
368
P3
bit3
354
206
108
300C

FIG. 22

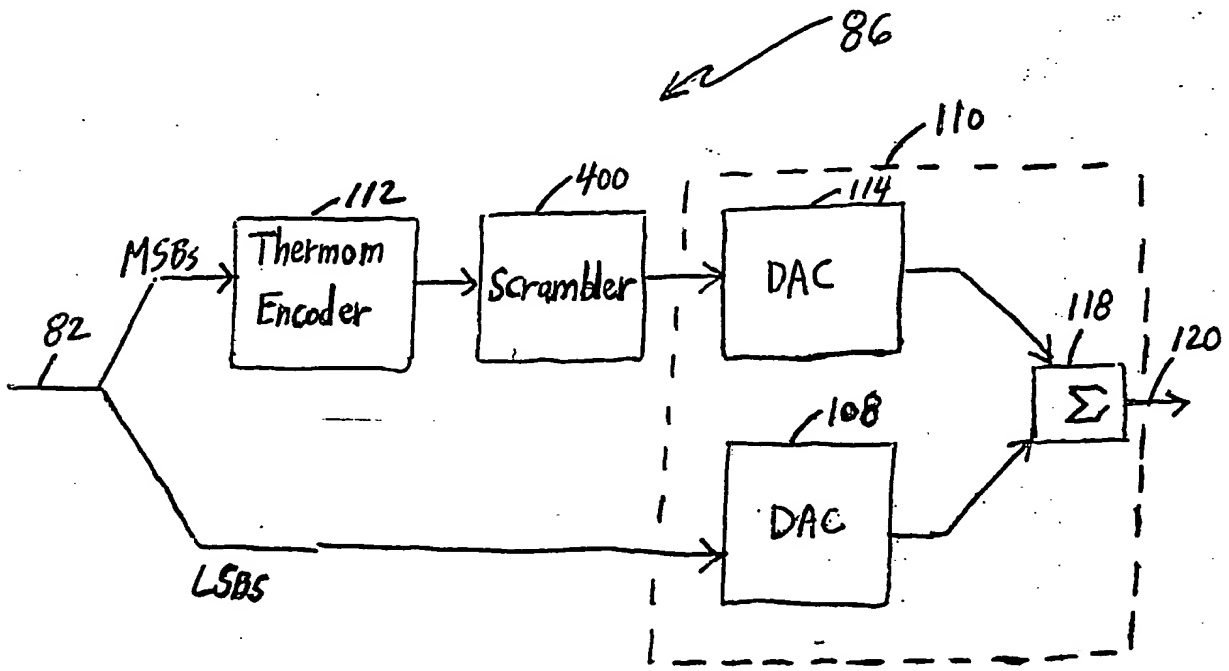

86
110
112
400
114
MSBs
Thermom Encoder
Scrambler
DAC
82
118
120
Σ
108
DAC
LSBs

FIG. 23

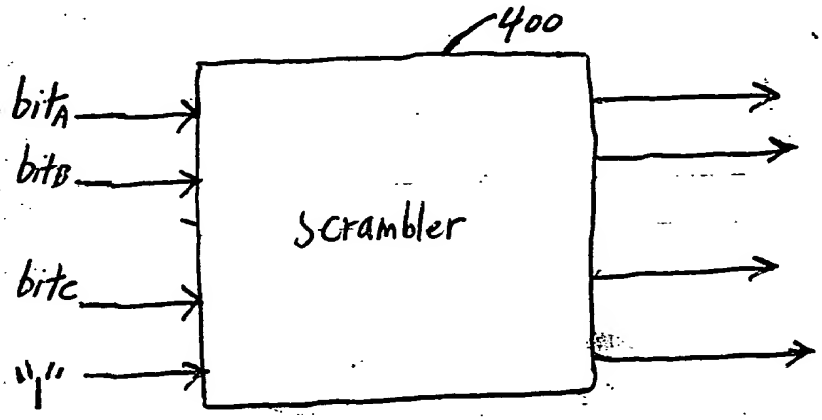


FIG 24

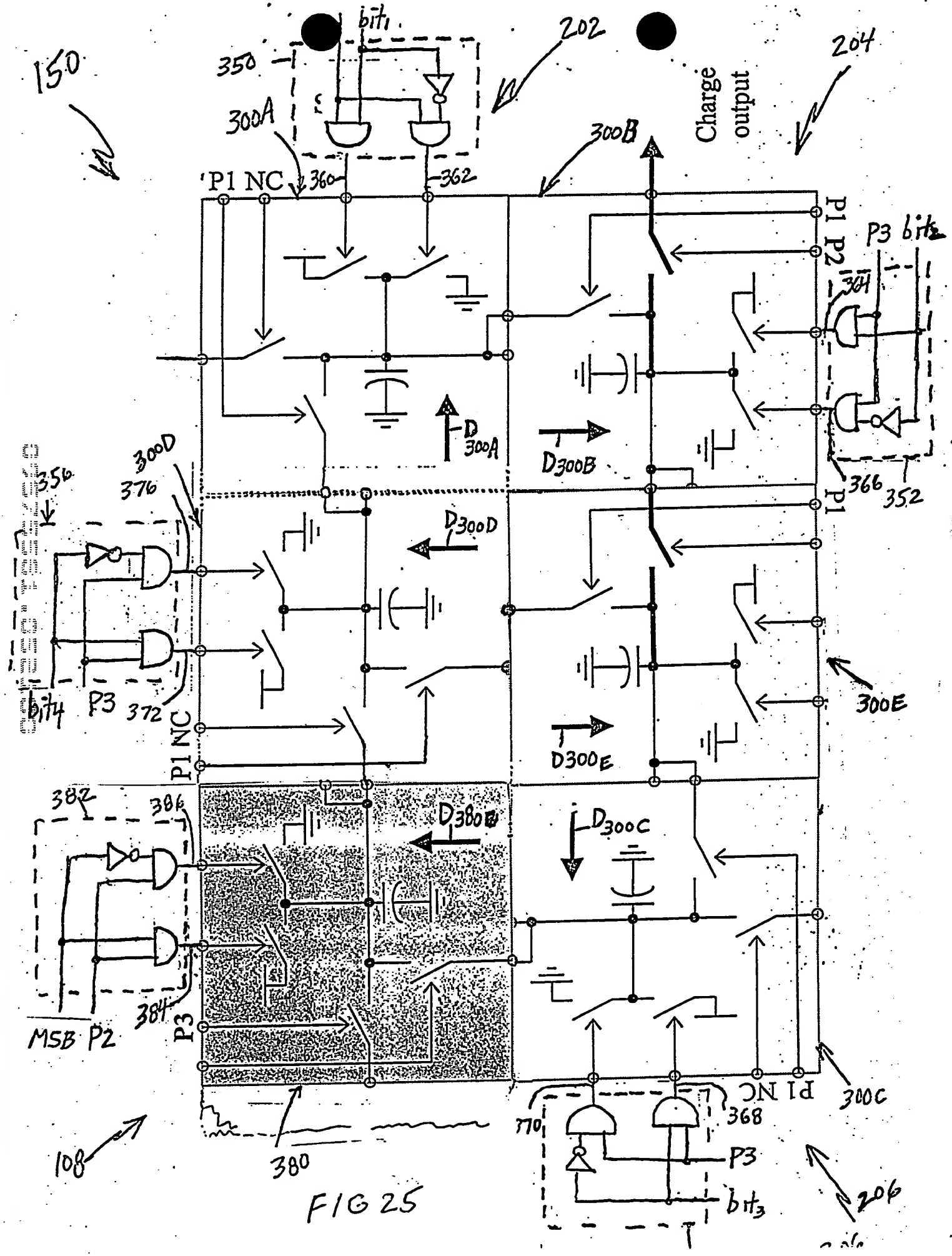

150
bit1
350
202
204
300A
300B
Charge output
P1 NC
360
362
P1 P2
P3 bit2
361
D300A
D300B
366
352
P1
300D
376
356
D300D
bit4
P3
372
300E
P1 NC
D300E
382
386
D380
D300C
MSB P2
384
P3
P1 NC
300C
368
370
P3
bit3
206
108
380

FIG 25

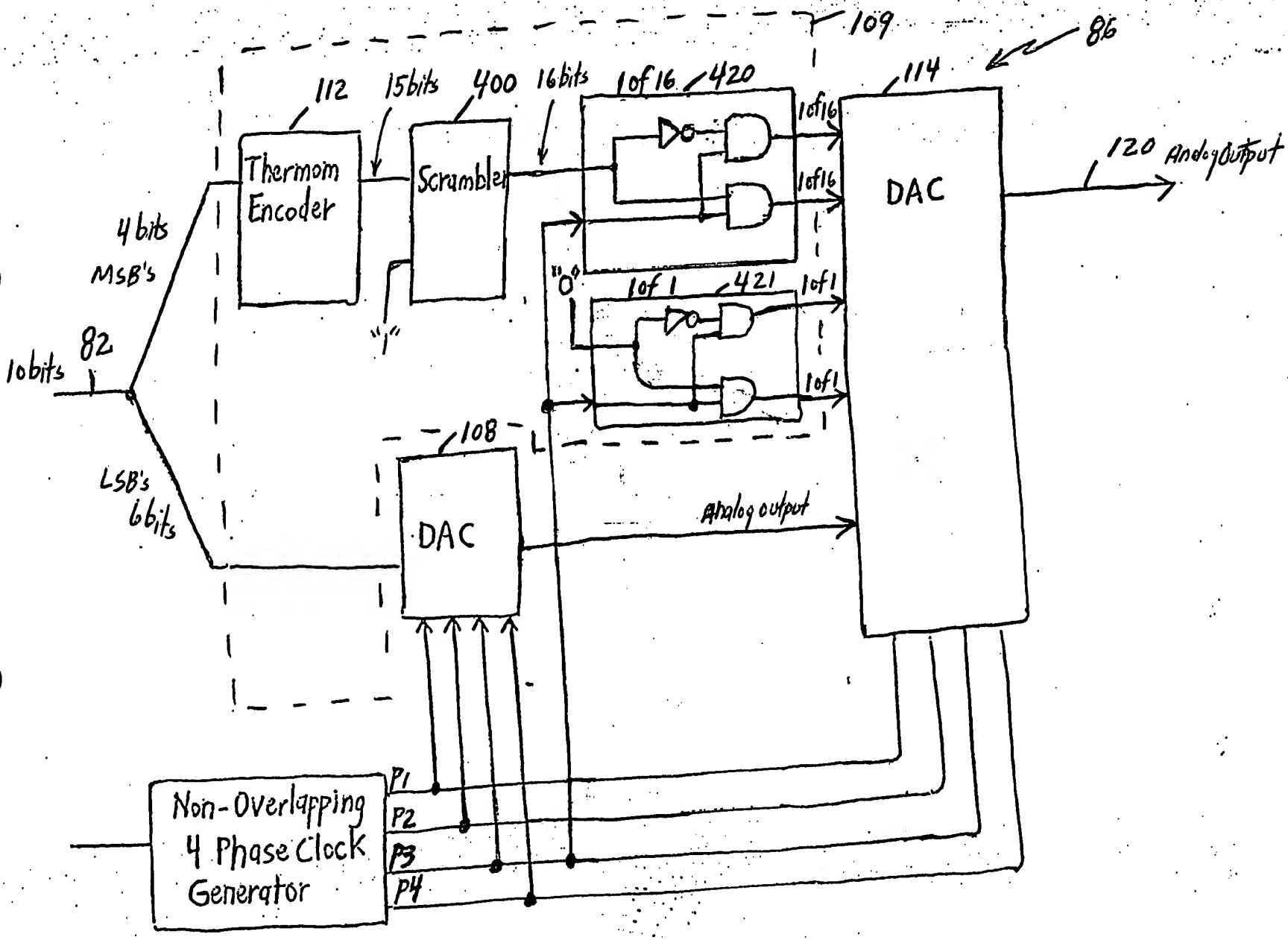

109
86
112
15bits
400
16bits
1of16
420
114
Thermom Encoder
Scrambler
1of16
1of16
DAC
120 Analog output
4 bits
MSB's
"0"
1of1
421
1of1
1of1
10bits
82
108
LSB's
6bits
DAC
Analog output
Non-Overlapping
4 Phase Clock
Generator
P1
P2
P3
P4

FIG 26

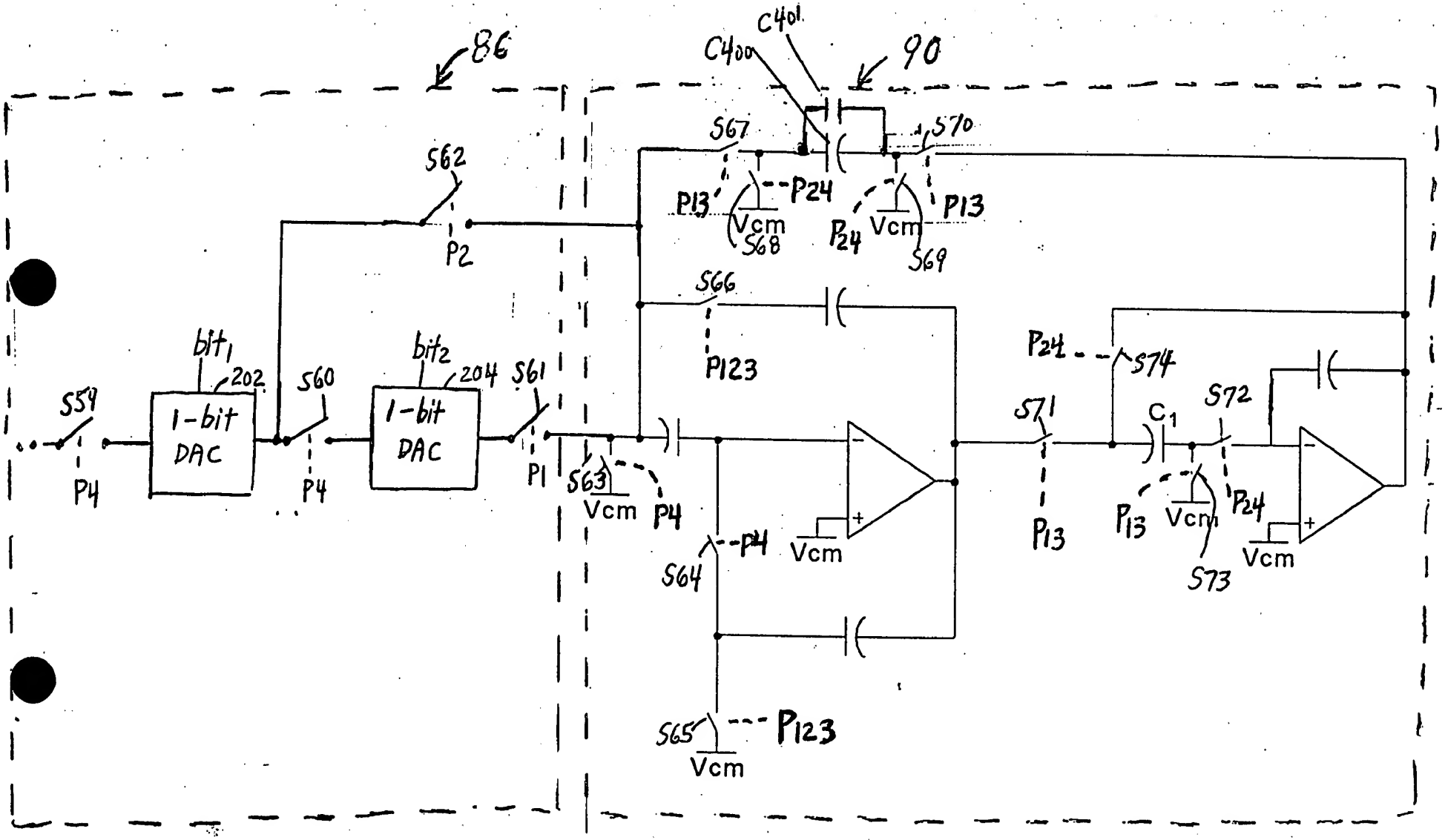

86
90
C401
C400
S67
S70
S62
P13
P24
Vcm
S68
P24
Vcm
P13
S69
P2
S66
P123
bit1
202
bit2
204
S59
S60
S61
1-bit DAC
1-bit DAC
P4
P4
P1
S63
Vcm
P4
S64
P4
Vcm
P24
S74
S71
C1
S72
P13
P13
Vcm
P24
Vcm
S73
S65
P123
Vcm

FIG 27

FIG 28A

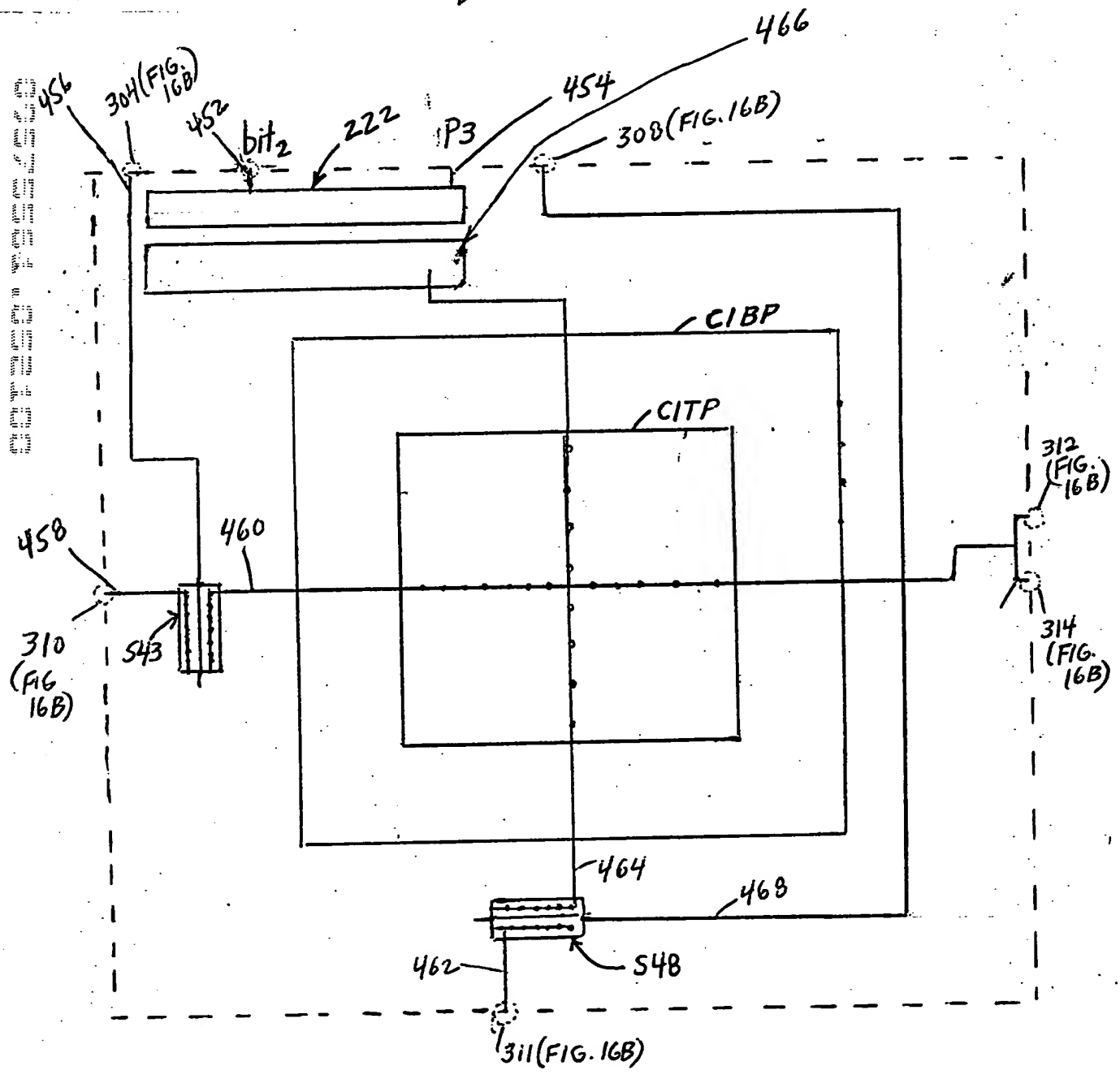
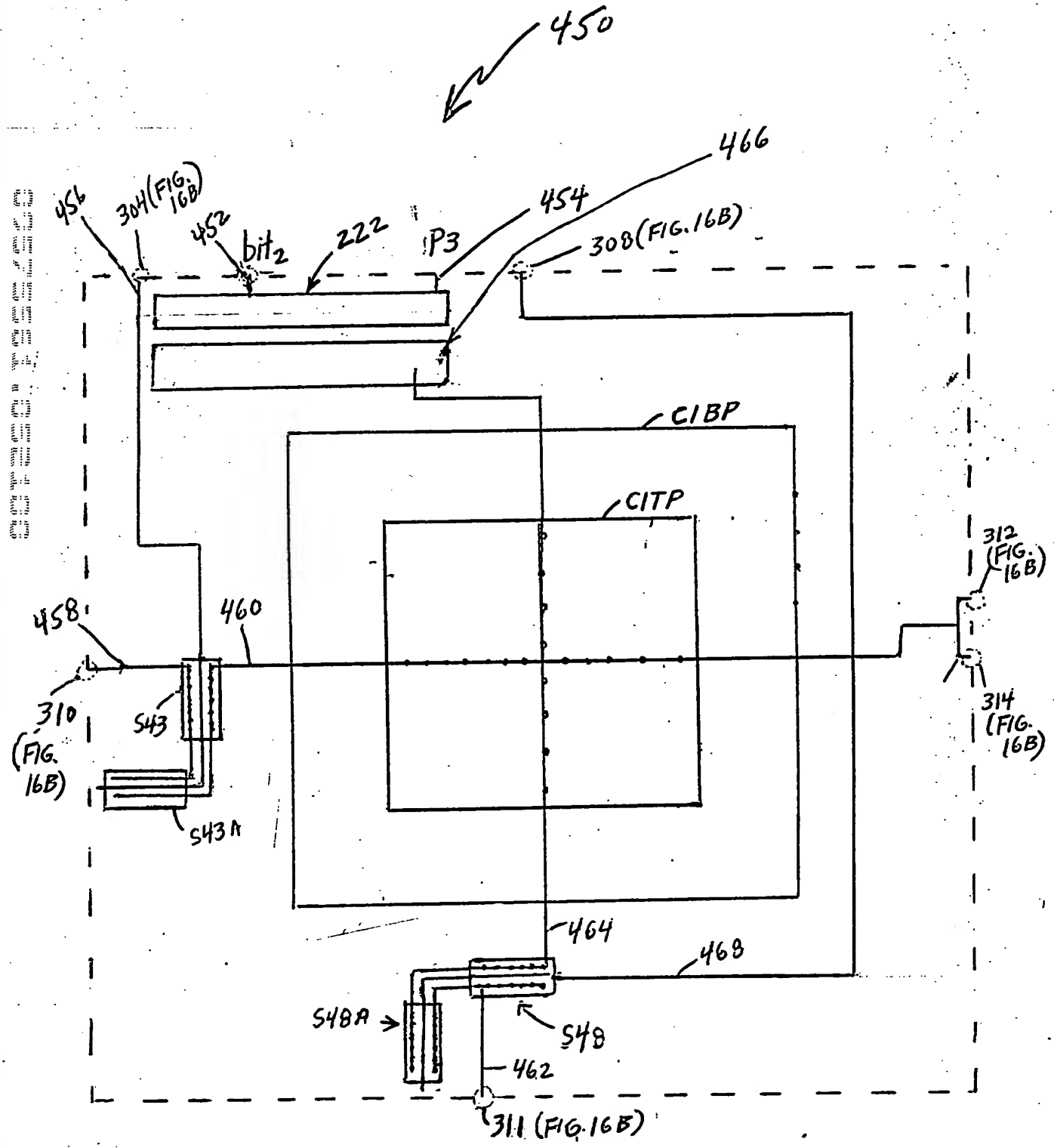

450
466
456
304(FIG. 16B)
452
bit2
222
P3
454
308(FIG. 16B)
CIBP
CITP
312 (FIG. 16B)
458
460
310 (FIG 16B)
543
314 (FIG. 16B)
464
468
462
548
311(FIG. 16B)

FIG 28B


450
466
456
304 (FIG. 16B)
452
bit2
222
P3
454
308 (FIG. 16B)
CIBP
CITP
312 (FIG. 16B)
458
460
310 (FIG. 16B)
S43
S43A
314 (FIG. 16B)
464
468
S48A
S48
462
311 (FIG. 16B)

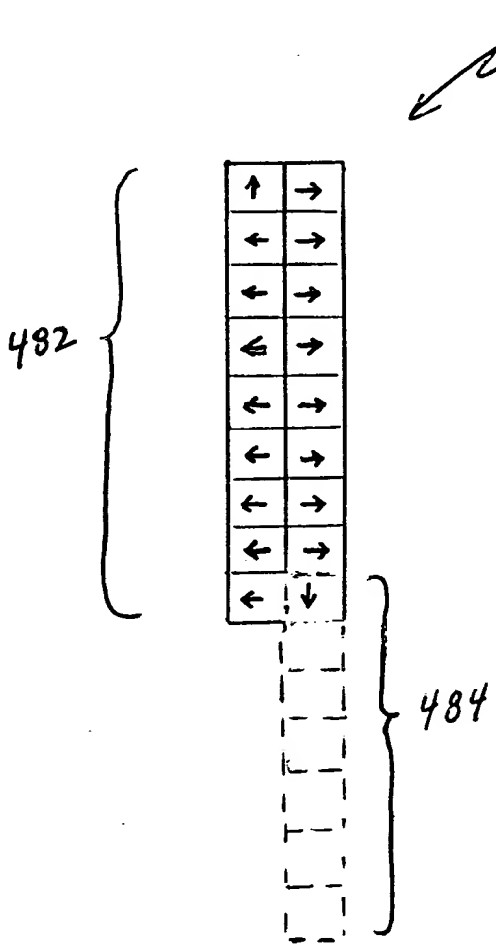


FIG. 29

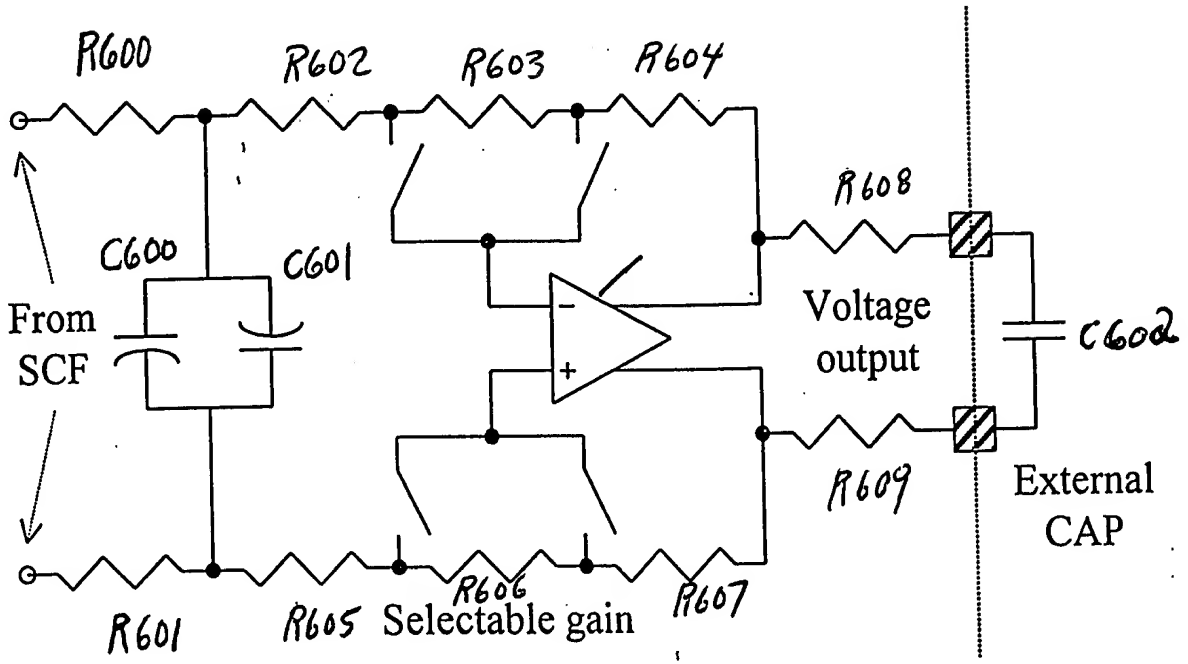

R600
R602
R603
R604
R608
C600
C601
From
SCF
Voltage
output
C602
R609
External
CAP
R601
R605
R606
Selectable gain
R607

FIG. 30

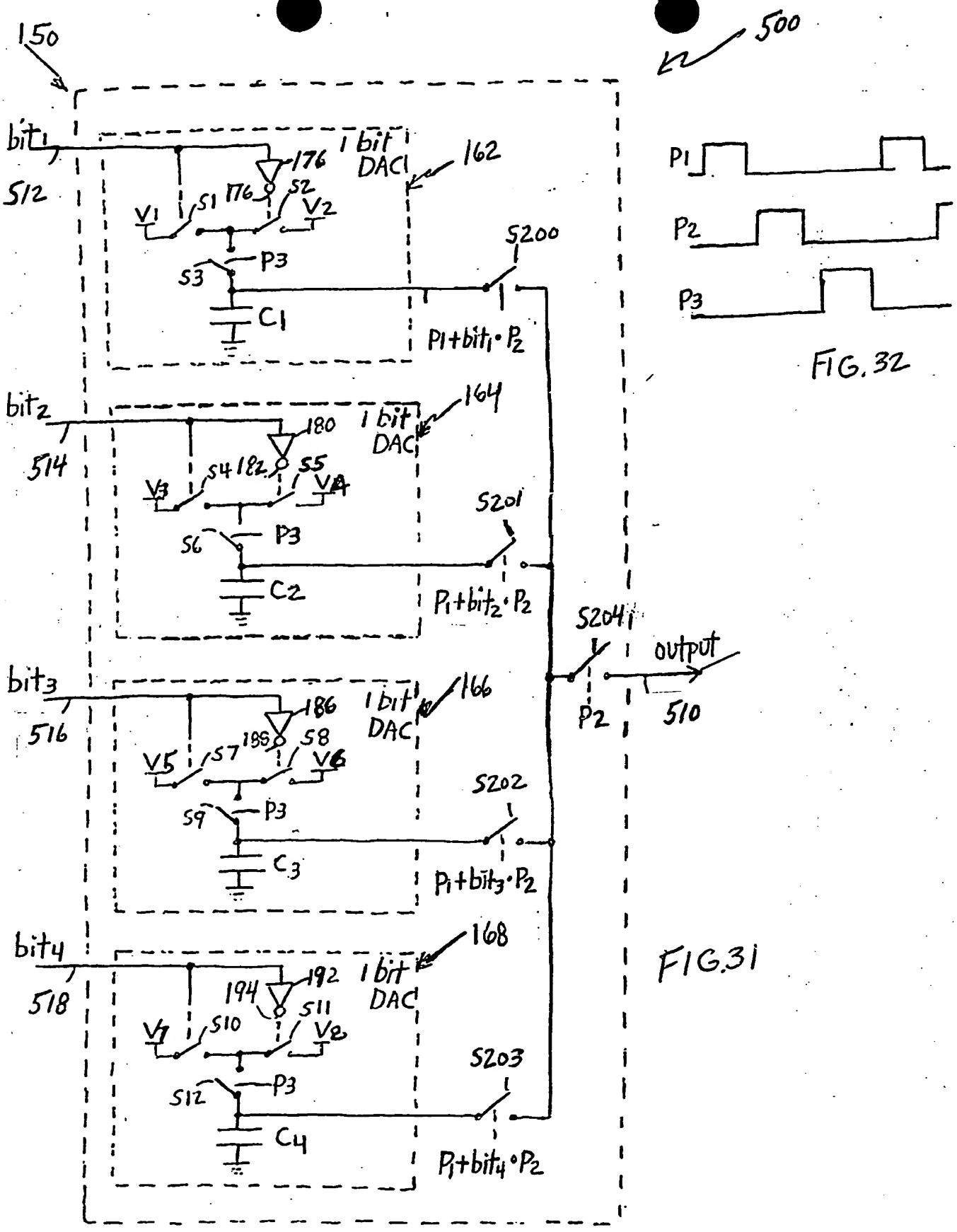

150
500
bit1
512
1 bit DAC
162
176
176
S1
S2
V1
V2
P3
S3
C1
S200
P1+bit1·P2
bit2
514
164
180
182
S4
S5
V3
V4
S201
P3
S6
C2
P1+bit2·P2
S204
output
510
P2
bit3
516
166
186
188
S7
S8
V5
V6
S202
P3
S9
C3
P1+bit3·P2
bit4
518
168
192
194
S10
S11
V7
V8
S203
P3
S12
C4
P1+bit4·P2

FIG.31

P1
P2
P3

FIG.32

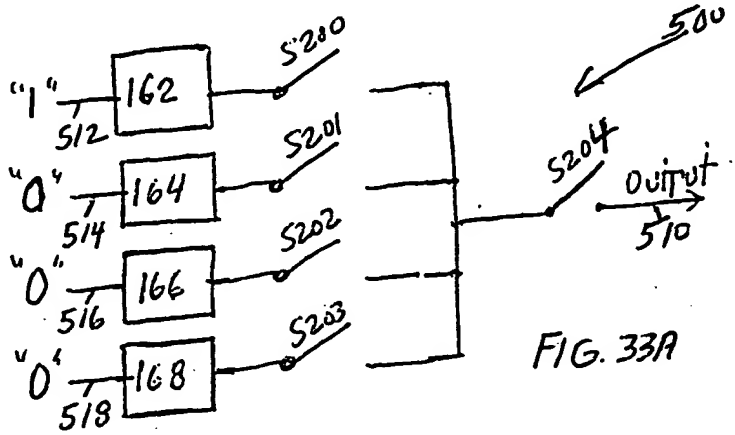


FIG. 33A

P1 "0"	V(C1) = Vref	Q(C1) = C*Vref
P2 "0"	V(C2) = 0	Q(C2) = 0
P3 "1"	V(C3) = 0	Q(C3) = 0
	V(C4) = 0	Q(C4) = 0

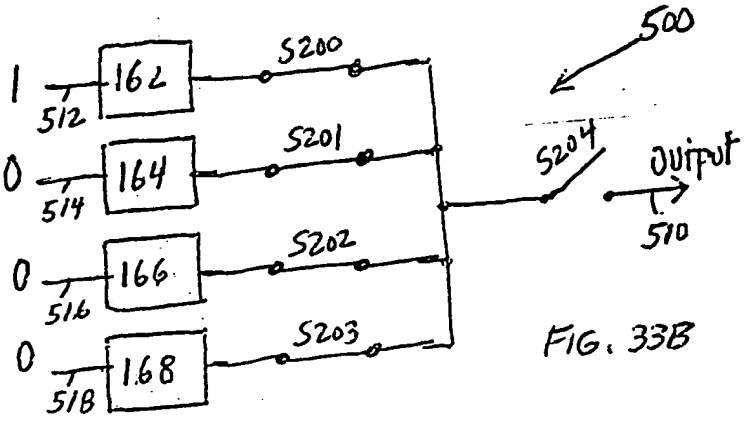


FIG. 33B

P1 = "1"	V(C1) = Vref/4	Q(C1) = C*Vref/4
P2 = "0"	V(C2) = Vref/4	Q(C2) = C*Vref/4
P3 = "0"	V(C3) = Vref/4	Q(C3) = C*Vref/4
	V(C4) = Vref/4	Q(C4) = C*Vref/4

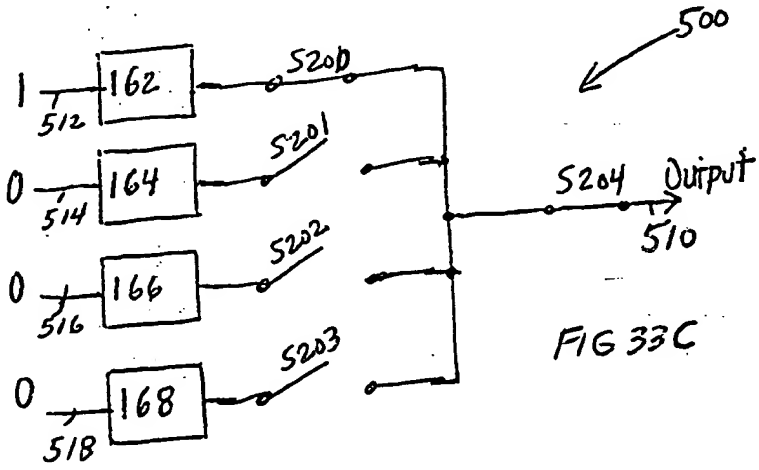


FIG 33C

P1 = "0"	V(C1) = Vref/4	Q(C1) = C*Vref/4
P2 = "1"	V(C2) = Vref/4	Q(C2) = C*Vref/4
P3 = "0"	V(C3) = Vref/4	Q(C3) = C*Vref/4
	V(C4) = Vref/4	Q(C4) = C*Vref/4

Q delivered to output terminal is Q(C1) = C*Vref/4

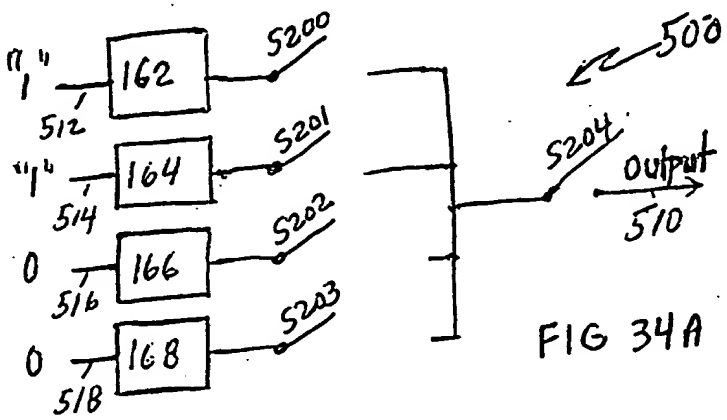


FIG 34A

P1 "0"	$V(C_1) = V_{ref}$	$Q(C_1) = C * V_{ref}$
P2 "0"	$V(C_2) = V_{ref}$	$Q(C_2) = C * V_{ref}$
P3 "1"	$V(C_3) = 0$	$Q(C_3) = 0$
	$V(C_4) = 0$	$Q(C_4) = 0$

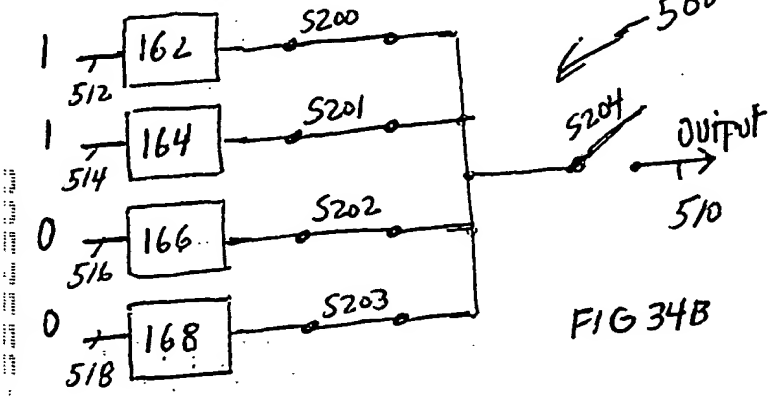


FIG 34B

P1 = "1"	$V(C_1) = V_{ref}/2$	$Q(C_1) = C * V_{ref}/2$
P2 = "0"	$V(C_2) = V_{ref}/2$	$Q(C_2) = C * V_{ref}/2$
P3 = "0"	$V(C_3) = V_{ref}/2$	$Q(C_3) = C * V_{ref}/2$
	$V(C_4) = V_{ref}/2$	$Q(C_4) = C * V_{ref}/2$

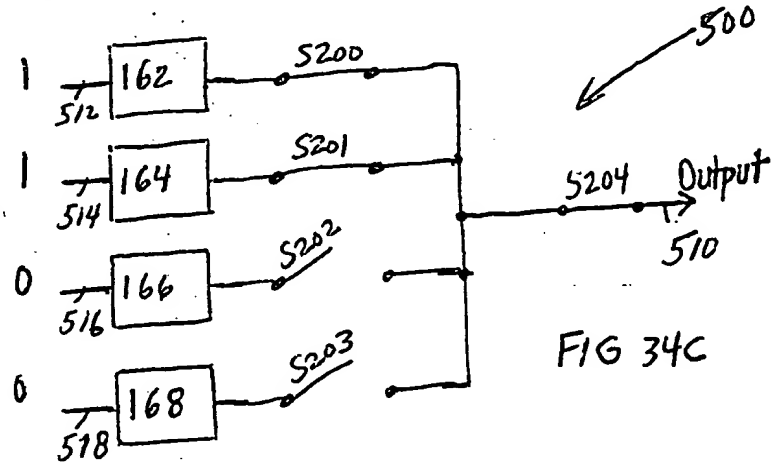


FIG 34C

P1 = "0"	$V(C_1) = V_{ref}/2$	$Q(C_1) = C * V_{ref}/2$
P2 = "1"	$V(C_2) = V_{ref}/2$	$Q(C_2) = C * V_{ref}/2$
P3 = "0"	$V(C_3) = V_{ref}/2$	$Q(C_3) = C * V_{ref}/2$
	$V(C_4) = V_{ref}/2$	$Q(C_4) = C * V_{ref}/2$

Q delivered to output terminal is $Q(C_1) + Q(C_2) =$

$C * V_{ref}/2 + C * V_{ref}/2 =$

$C * V_{ref}$

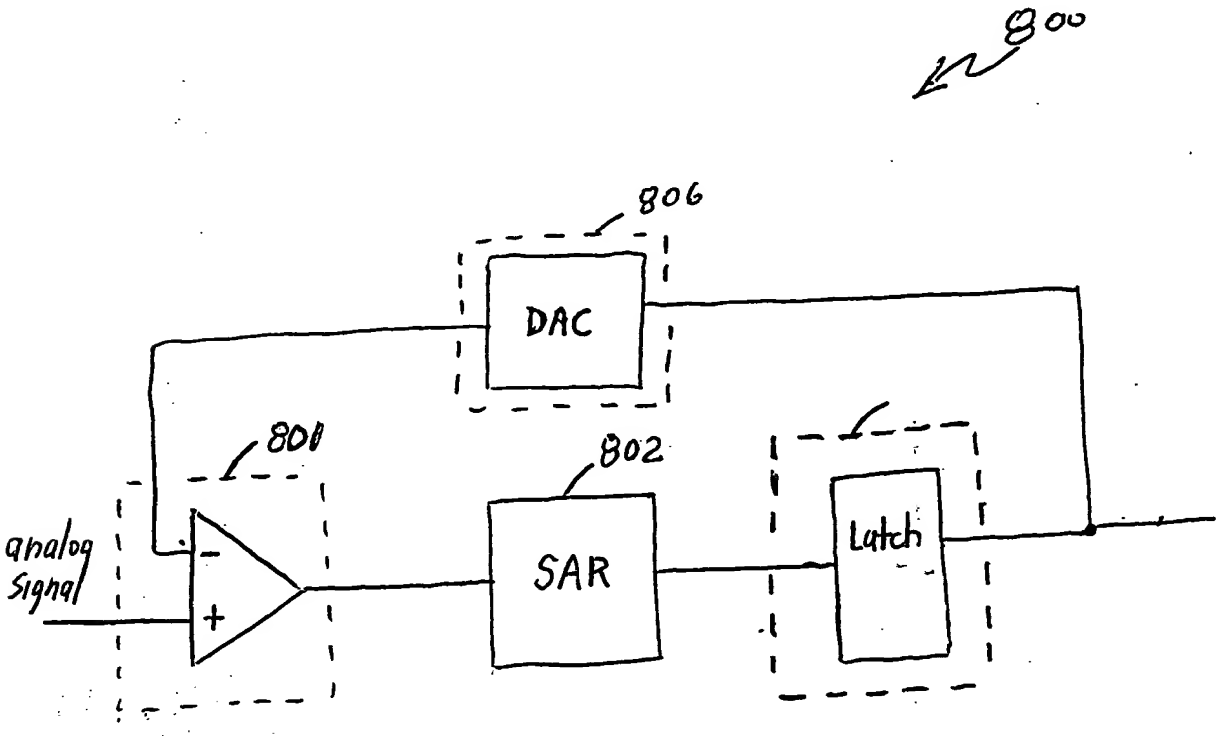


FIG. 35